

# Enrico/Caruso 15" UMA Schematics Document

## rPGA988A Mobile Arrandale

Intel Ibex Peak-M

2011-04-22

REV : A00

*DY : Nopop Component*  
*HDMI : Pop for HDMI function*  
*No\_HDMI : Pop for NO HDMI function*  
*10/100 : Pop for 10/100 LAN*  
*GIGA : Pop for GIGA LAN*  
*Surge : Pop for surge option*  
*G709 : Pop G709 thermal solution*  
*INS : Pop for Inspiron series ID*  
*VOS : Pop for Vostro series ID*  
*S3 : Pop for S3 power reduction*  
*Normal : Pop for NO S3 power reduction*

DV15 CP UMA second



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Title

**Cover Page**

Size  
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Document Number

**Enrico/Caruso 15 CP**

Rev  
A00

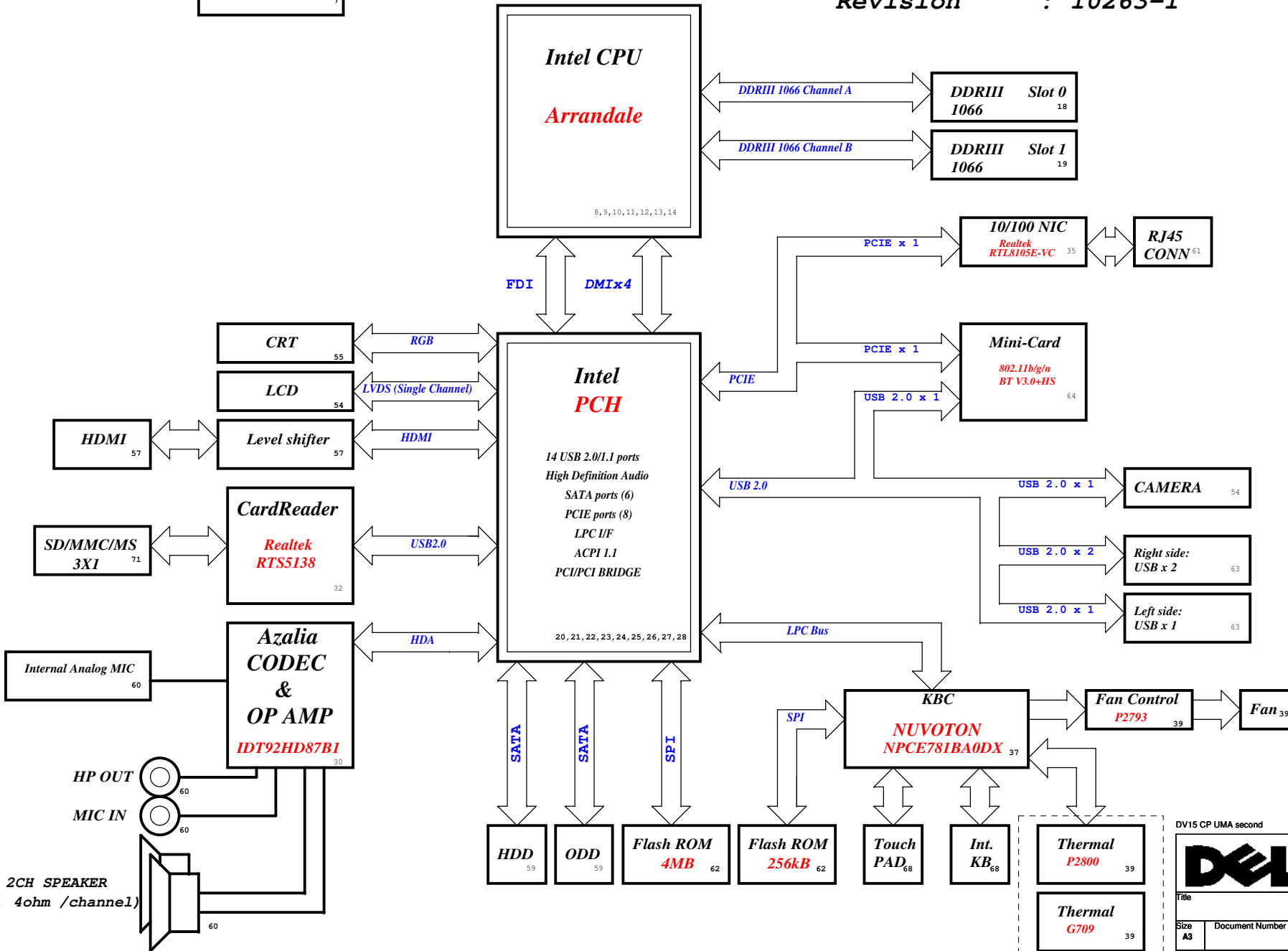
Date: Friday, April 22, 2011

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# DV15 Calpella UMA Block Diagram

Clock Generator  
**SLG8SP595**

Project code : 91.4IP01.001  
PCB P/N : 48.4IP01.011  
Revision : 10263-1



MAXIM CHARGER	
BQ24707 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC	
TPS51123 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +3.3V_ALW +5V_ALW +15V_ALW
CPU DC/DC	
ISL62882 47, 48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC	
RT8237A 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_CPU +1.05V_PCH
SYSTEM DC/DC	
RT8207 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +V_DDR_REF +0.75V_DDR_VTT
SYSTEM DC/DC	
APW7153B 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
SYSTEM DC/DC	
TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE
SYSTEM DC/DC	
Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_CPU +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top L2: GND L3: Signal L4: Signal L5: VCC L6: Bottom	

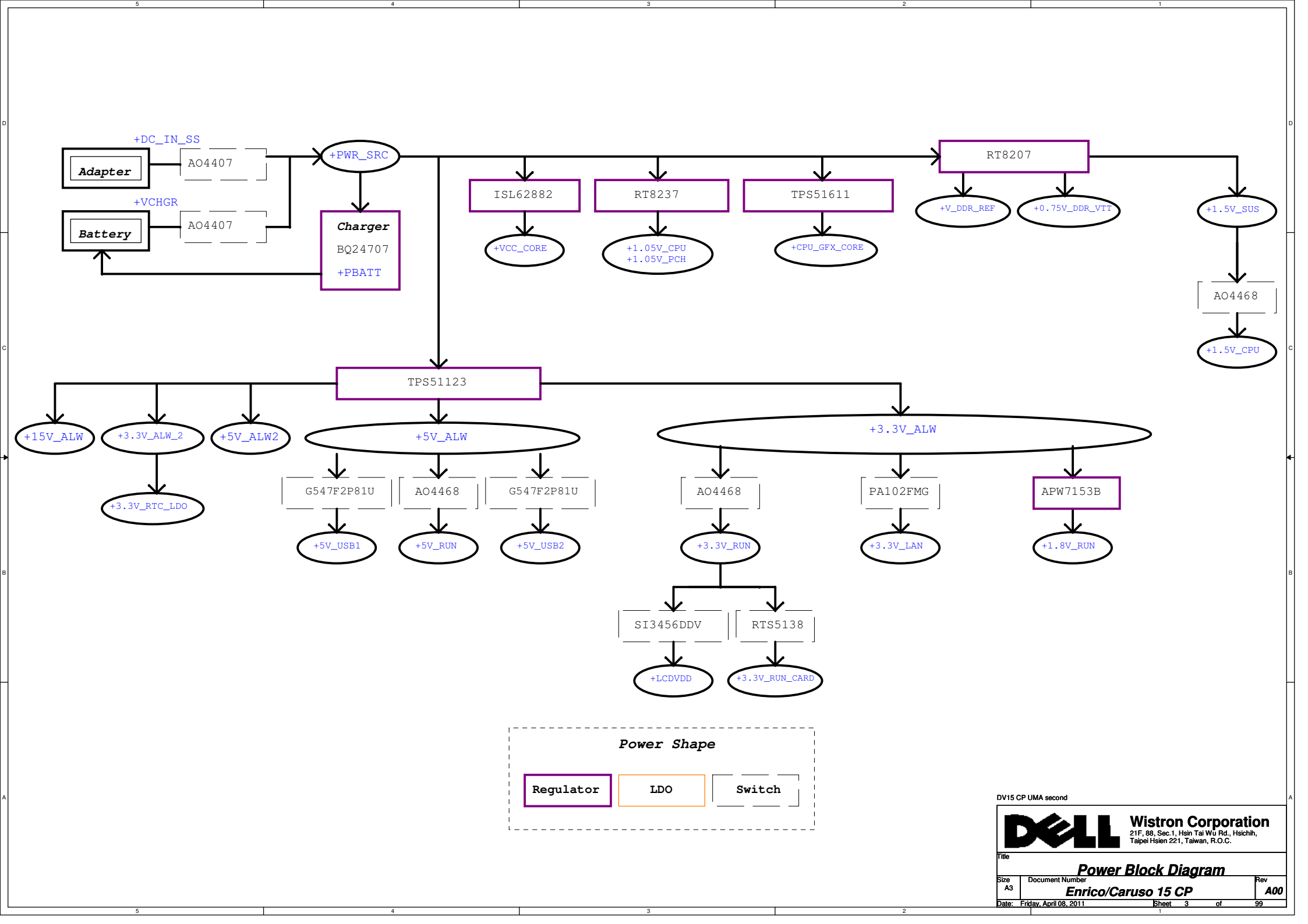
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Title: **Block Diagram**

Size: A3 Document Number: **Enrico/Caruso 15 CP** Rev: **A00**

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**Power Block Diagram**

Size  
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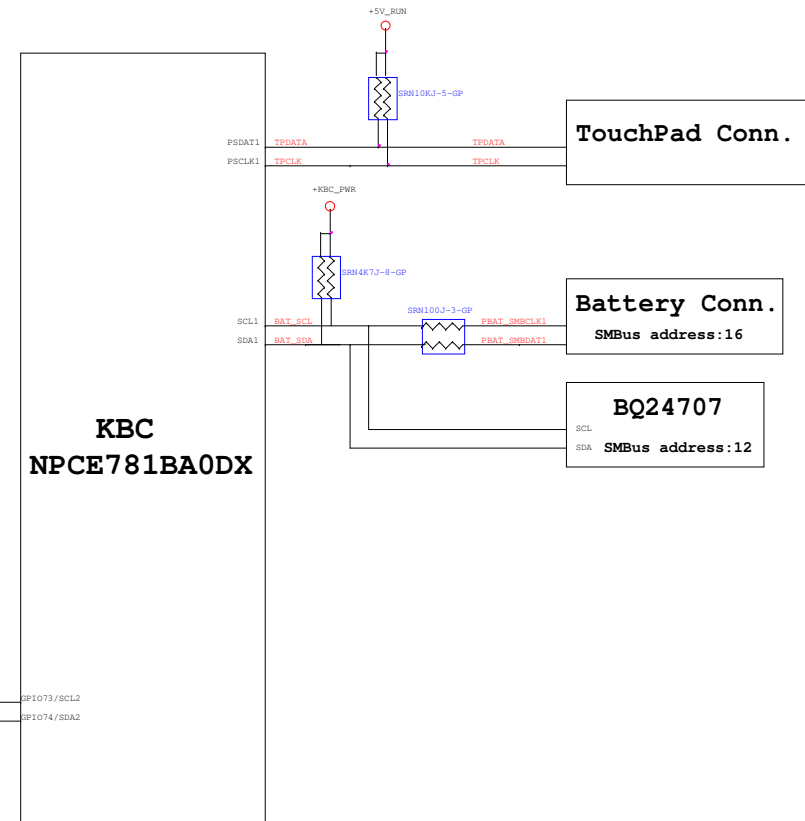
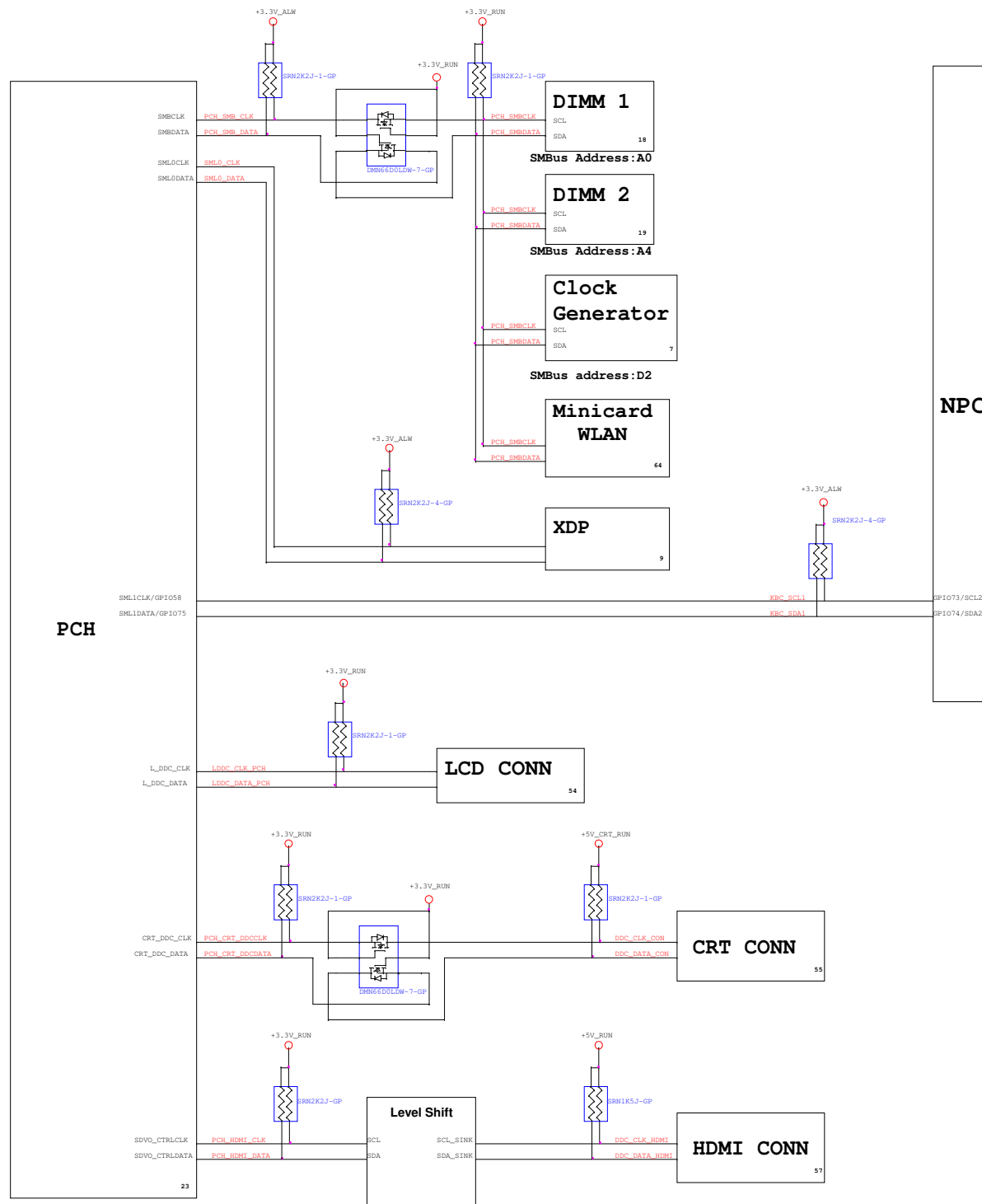
Rev

**A00**

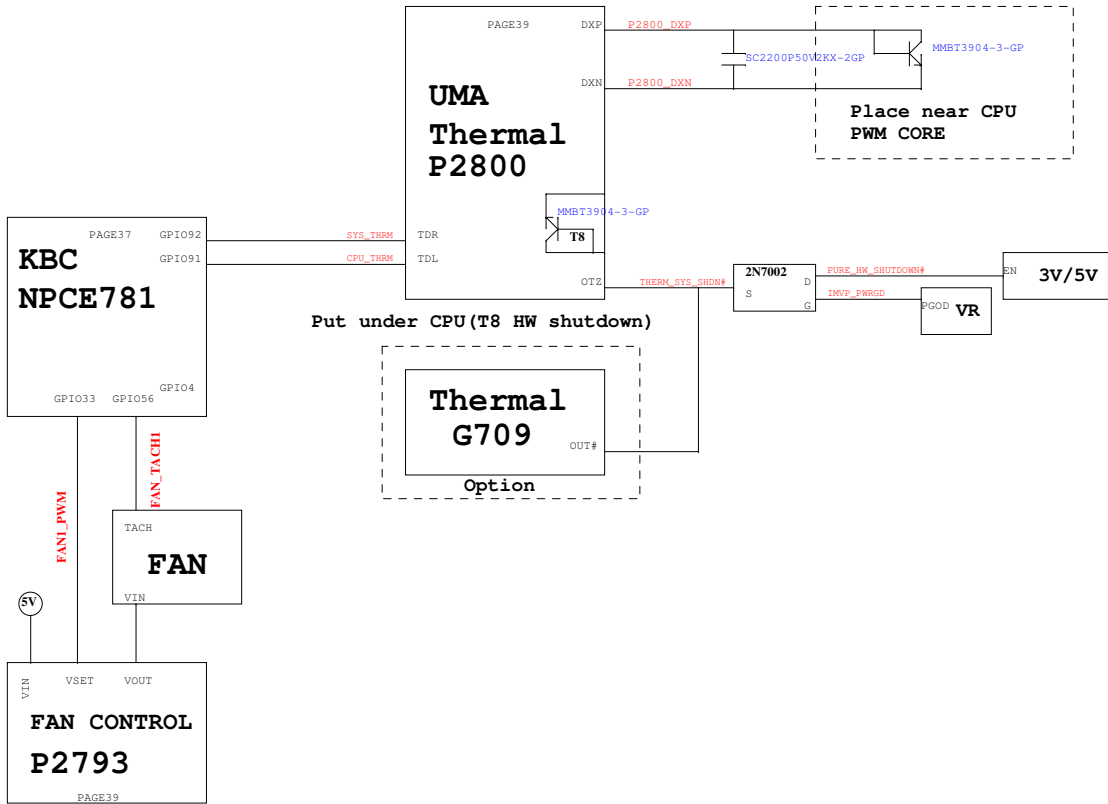
Date: Friday, April 08, 2011

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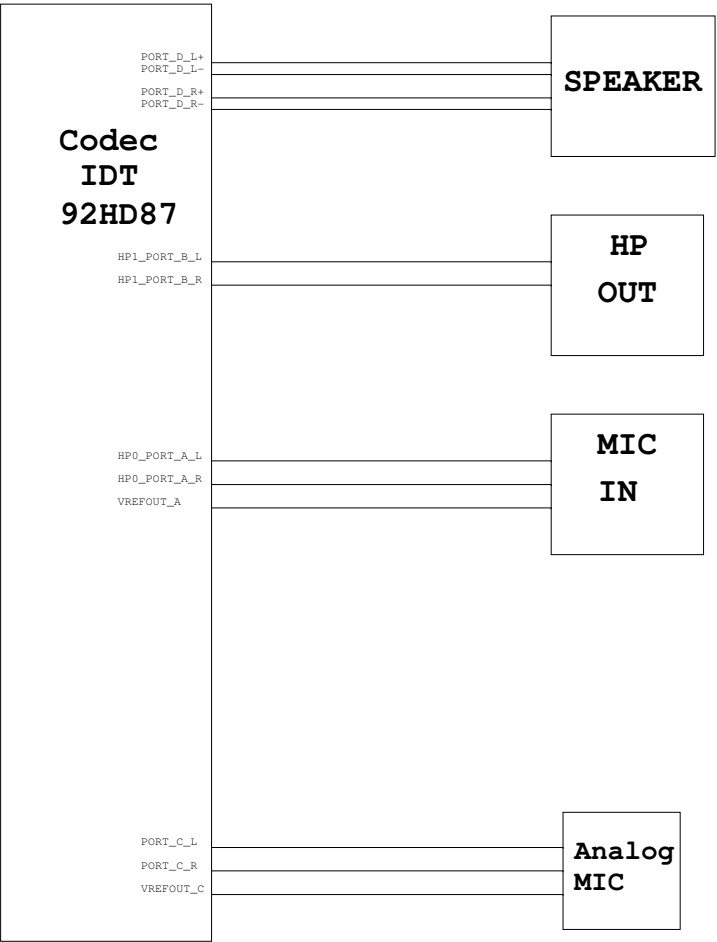
### KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



## PCH Strapping

Calpella Schematic Checklist Rev.0\_7

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-k $\Omega$ - 10-k $\Omega$ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-k $\Omega$ weak pull-down resistor).
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b>
GNT0#, GNT1#/GPIO51	<b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required. <b>Boot from PCI:</b> Connect GNT1# to ground with 1-k $\Omega$ pull-down resistor. Leave GNT0# Floating. <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-k $\Omega$ pull-down resistor.
GNT2#/GPIO53	<b>Default - Internal pull-up.</b> <b>Low (0)</b> = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	<b>Default:</b> Do not pull low. <b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-k $\Omega$ pull-down resistor.
SPI_MOSI	<b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-k $\Omega$ weak pull-up resistor. <b>Disable iTPM:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-k $\Omega$ weak pull-up resistor. <b>Disable Danbury:</b> Connect to ground with 4.7-k $\Omega$ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. <b>High (1) :</b> Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

## PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

## USB Table

USB	
Pair	Device
0	X
1	USB1
2	USB2 (Ext I/O BD)
3	USB3 (Ext I/O BD)
4	X
5	X
6	X
7	X
8	X
9	WLAN + Bluetooth
10	CARD READER
11	CAMERA
12	X
13	X

## Processor Strapping

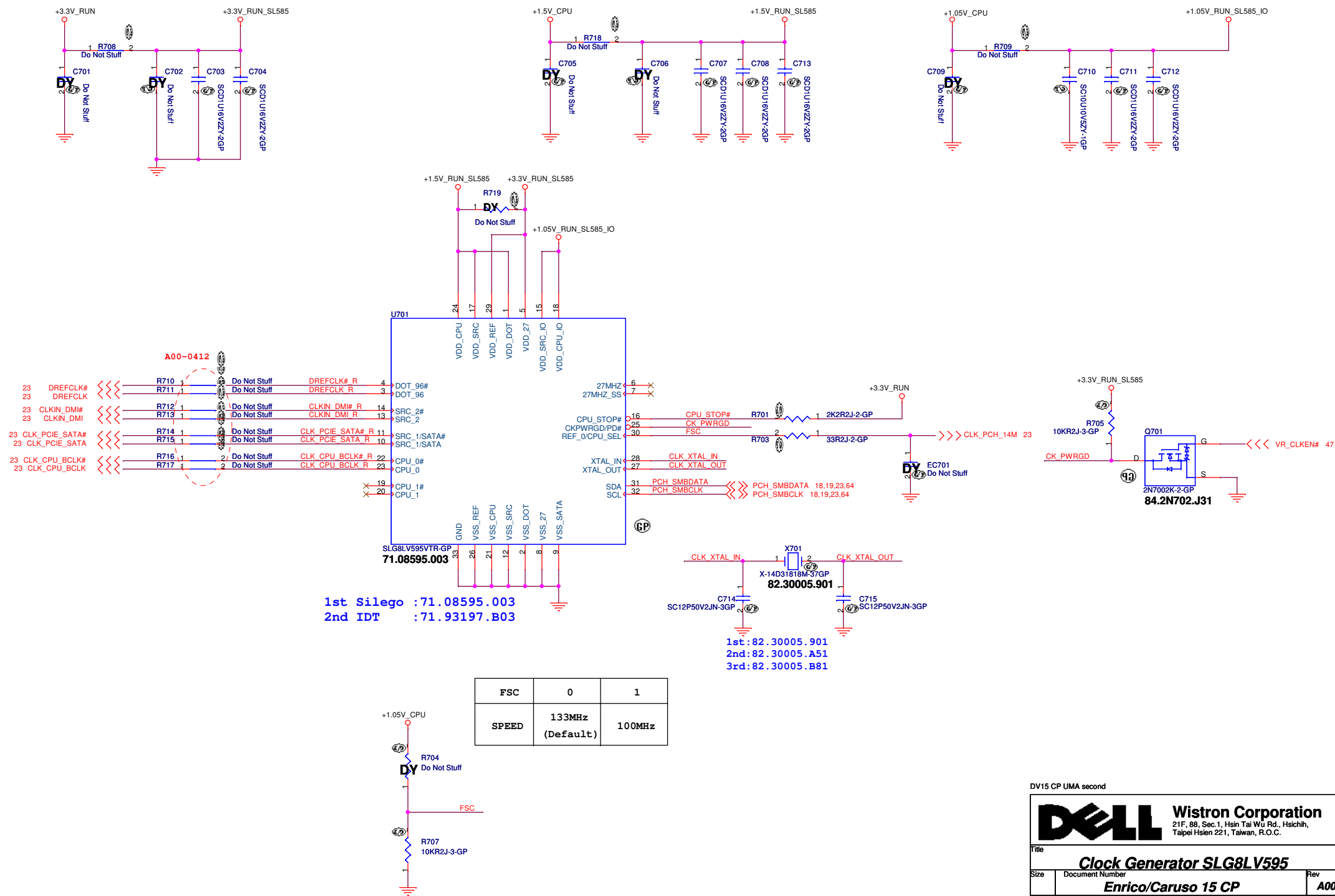
Calpella Schematic Checklist Rev.0\_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	<b>1:</b> Disabled - No Physical Display Port attached to Embedded DisplayPort. <b>0:</b> Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	<b>1:</b> Normal Operation. <b>0:</b> Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	<b>1:</b> Single PCI-Express Graphics <b>0:</b> Bifurcation enabled	1
CFG[7]	<b>Reserved - Temporarily used for early Clarksfield samples.</b>	<b>Clarksfield (only for early samples pre-ES1) -</b> Connect to GND with 3.01K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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<b>Table of Content</b>			
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**SSID = CLOCK**

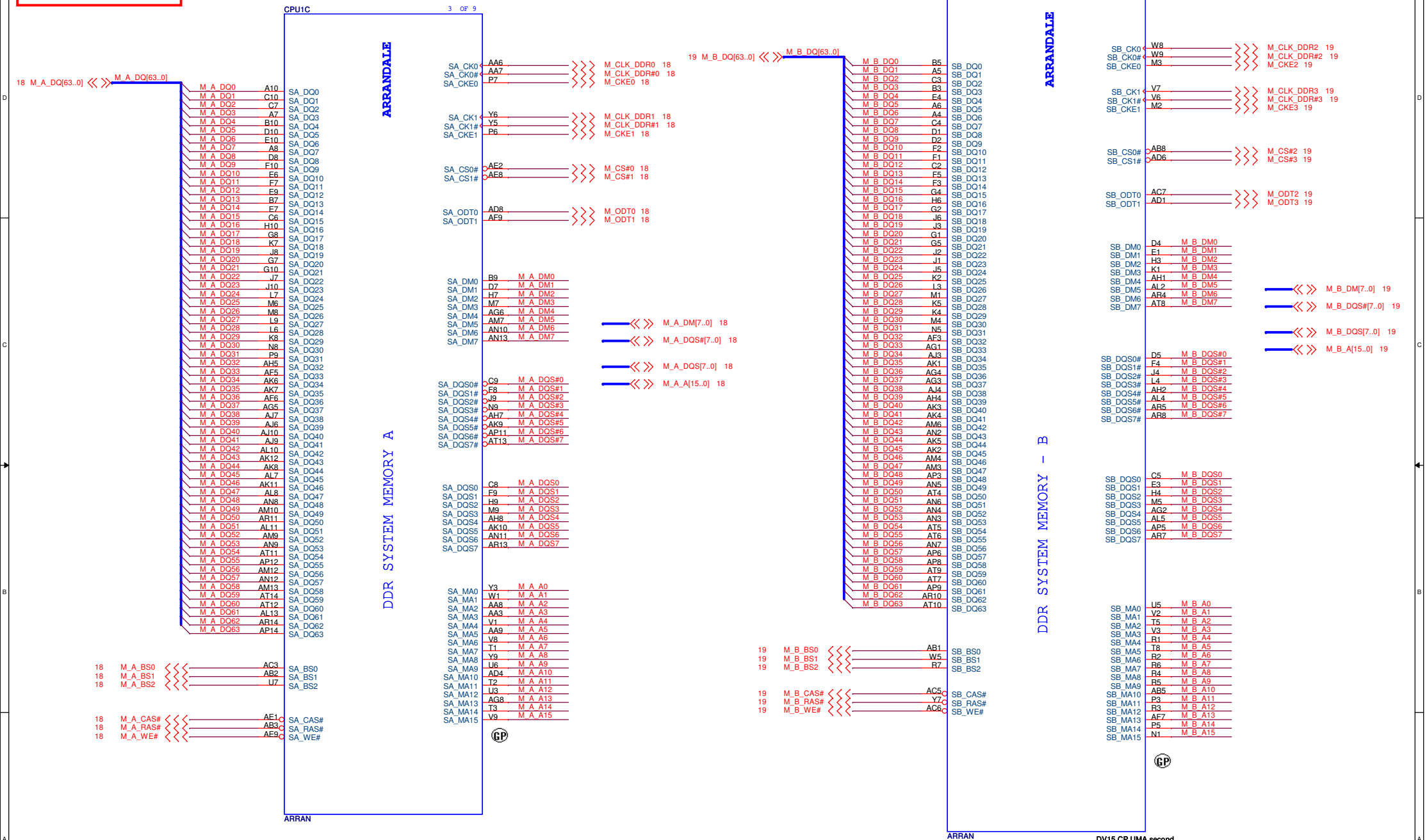


Title			
<b>CPU (PCIe/DMI/FDI)</b>			
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**SSID = CPU**



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**CPU (DDR)**

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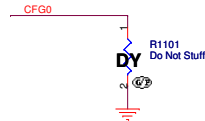
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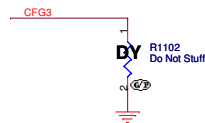
Rev

A00

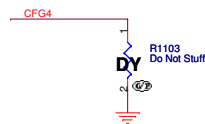
SSID = CPU



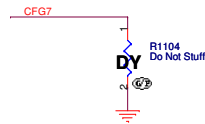
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



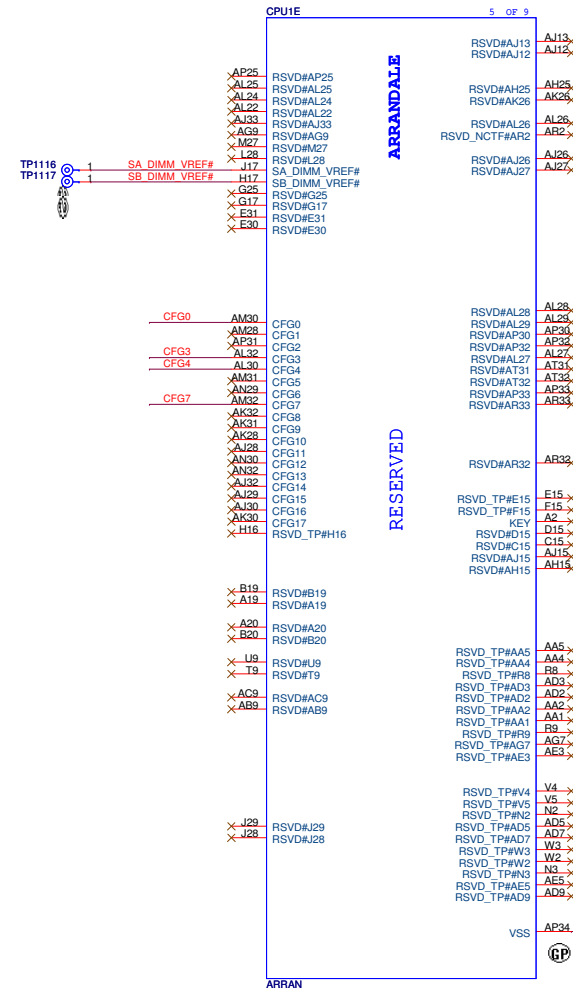
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.  Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



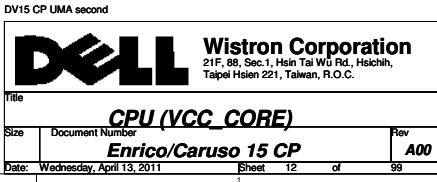
VSS (AP34) can be left NC is  
CRB implementation; EDS/DG  
recommendation to GND.

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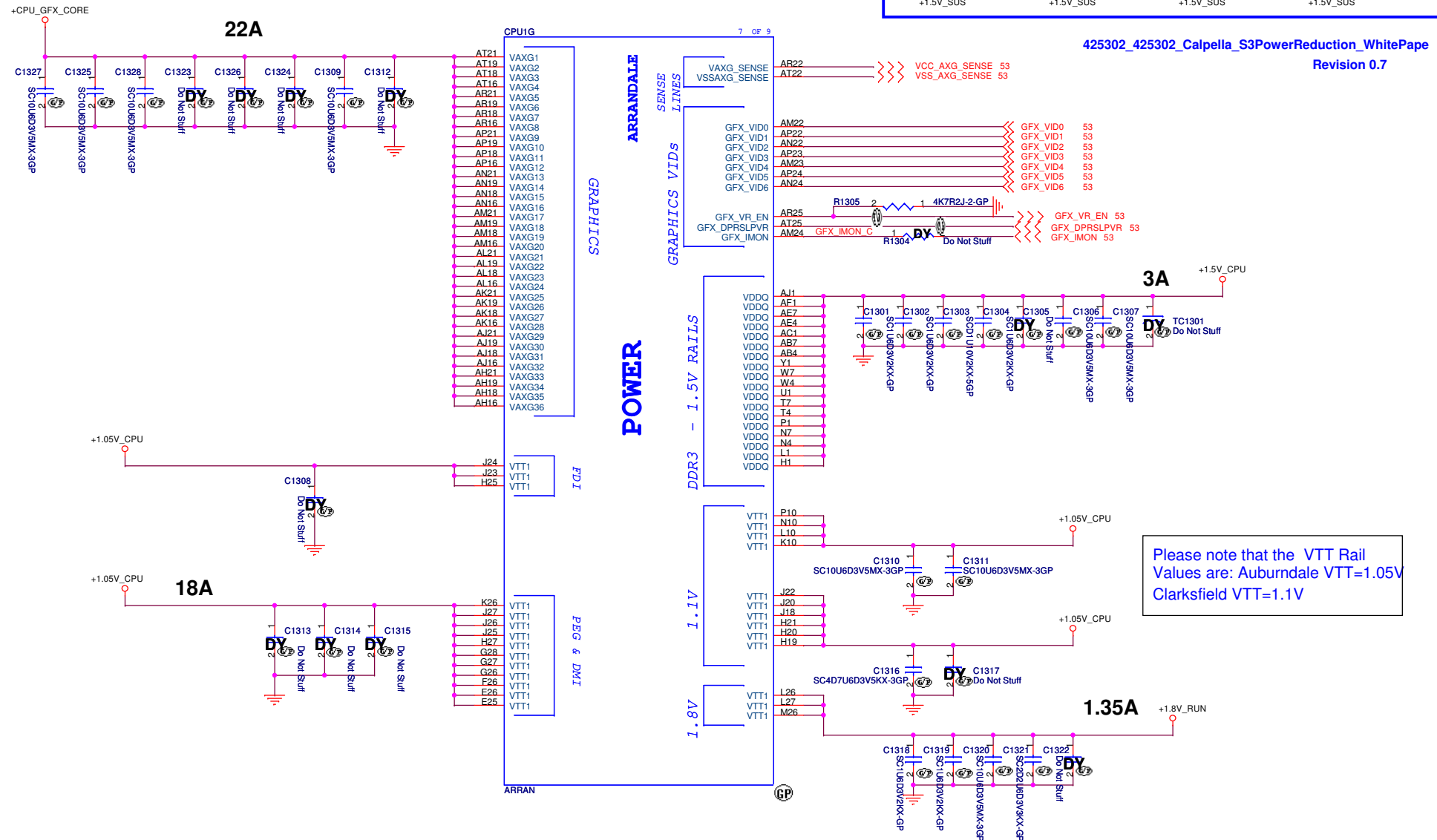


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CPU (RESERVED)		
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**SSID = CPU**



**SSID = CPU**

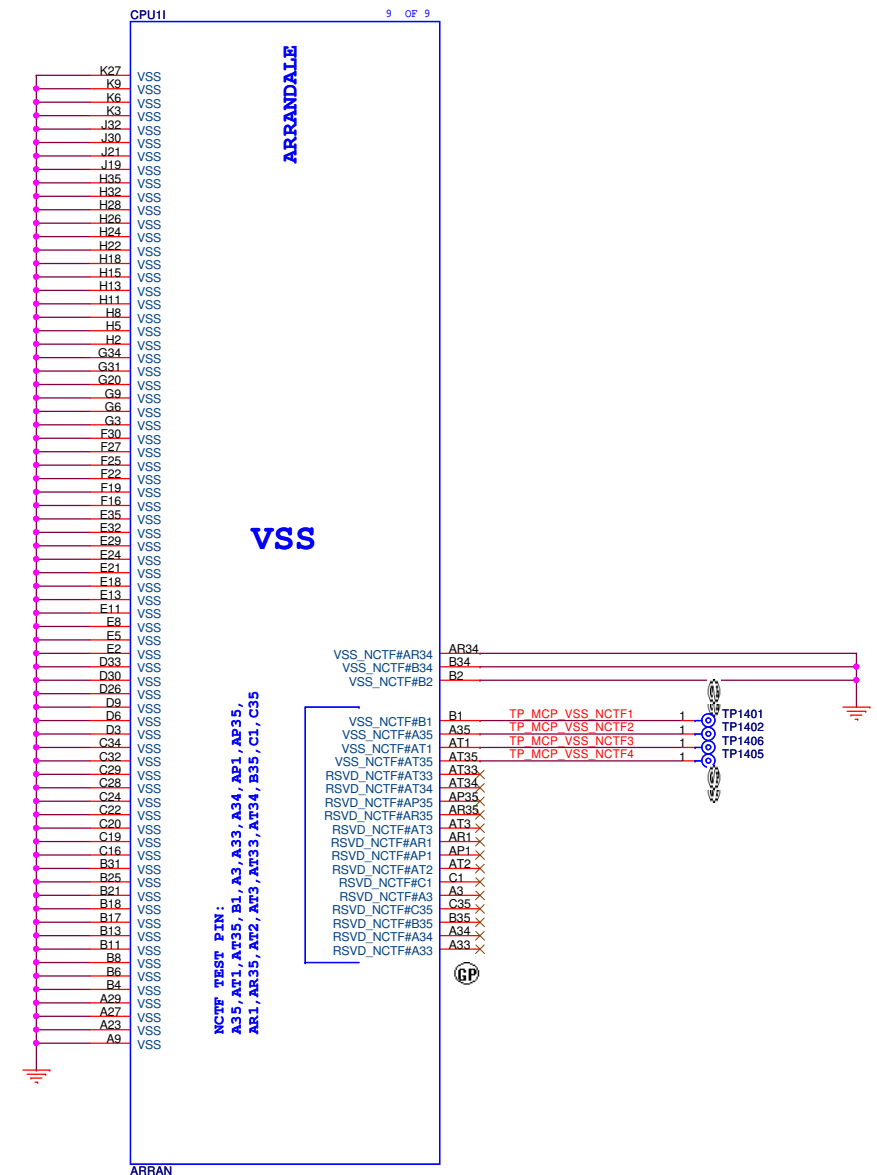
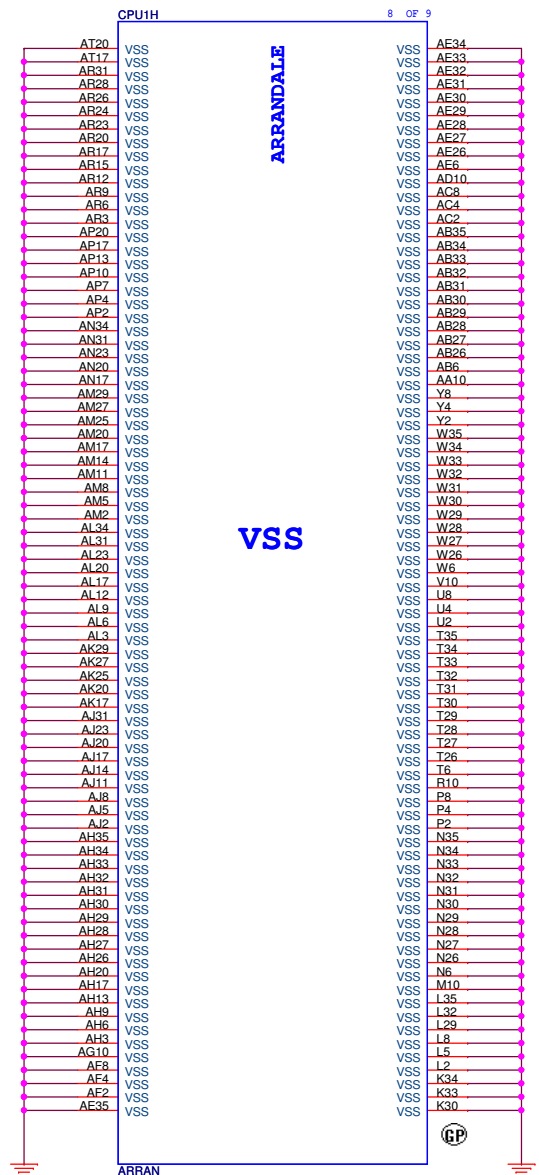


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Title			
<b>CPU (VCC GFXCORE)</b>			
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	<b>Enrico/Caruso 15 CP</b>	<b>A00</b>	
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SSID = CPU



NCT TEST PIN:  
A35, AT1, AT35, B1, A3, A33, A34, AP1, AP35,  
AR1, AR35, AT2, AT3, AT33, AT34, B35, C1, C35

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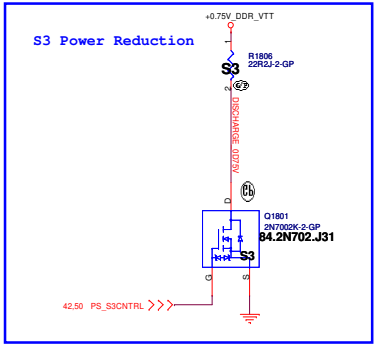
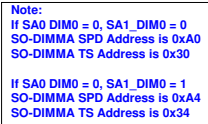
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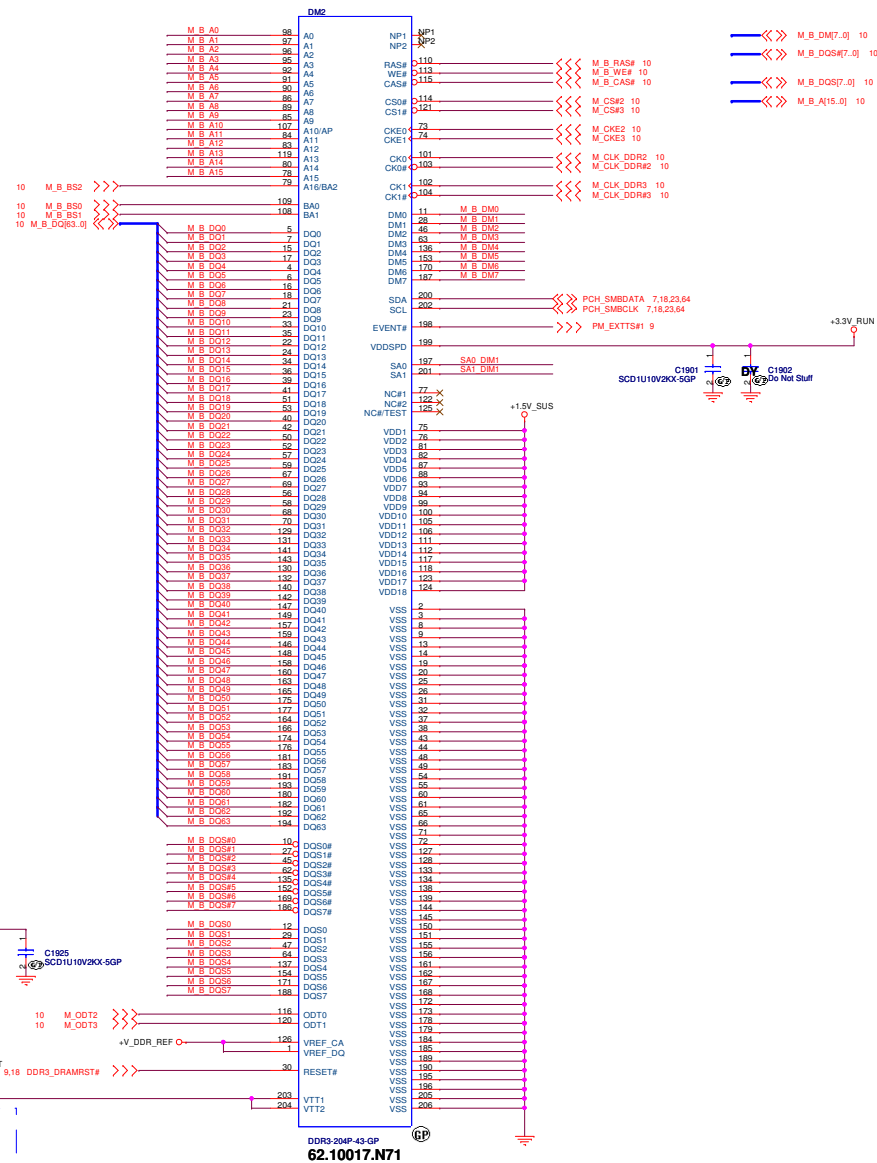
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**Reserved**

Place these caps  
close to VTT1 and  
VTT2.

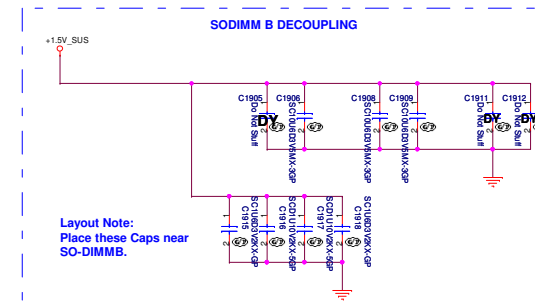
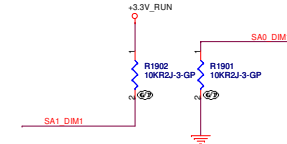


## SSID = MEMORY



**Note:**  
If SA0\_DIM1 = 0, SA1\_DIM1 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30

If SA0\_DIM1 = 0, SA1\_DIM1 = 1  
SO-DIMMA SPD Address is 0xA4  
SO-DIMMA TS Address is 0x34

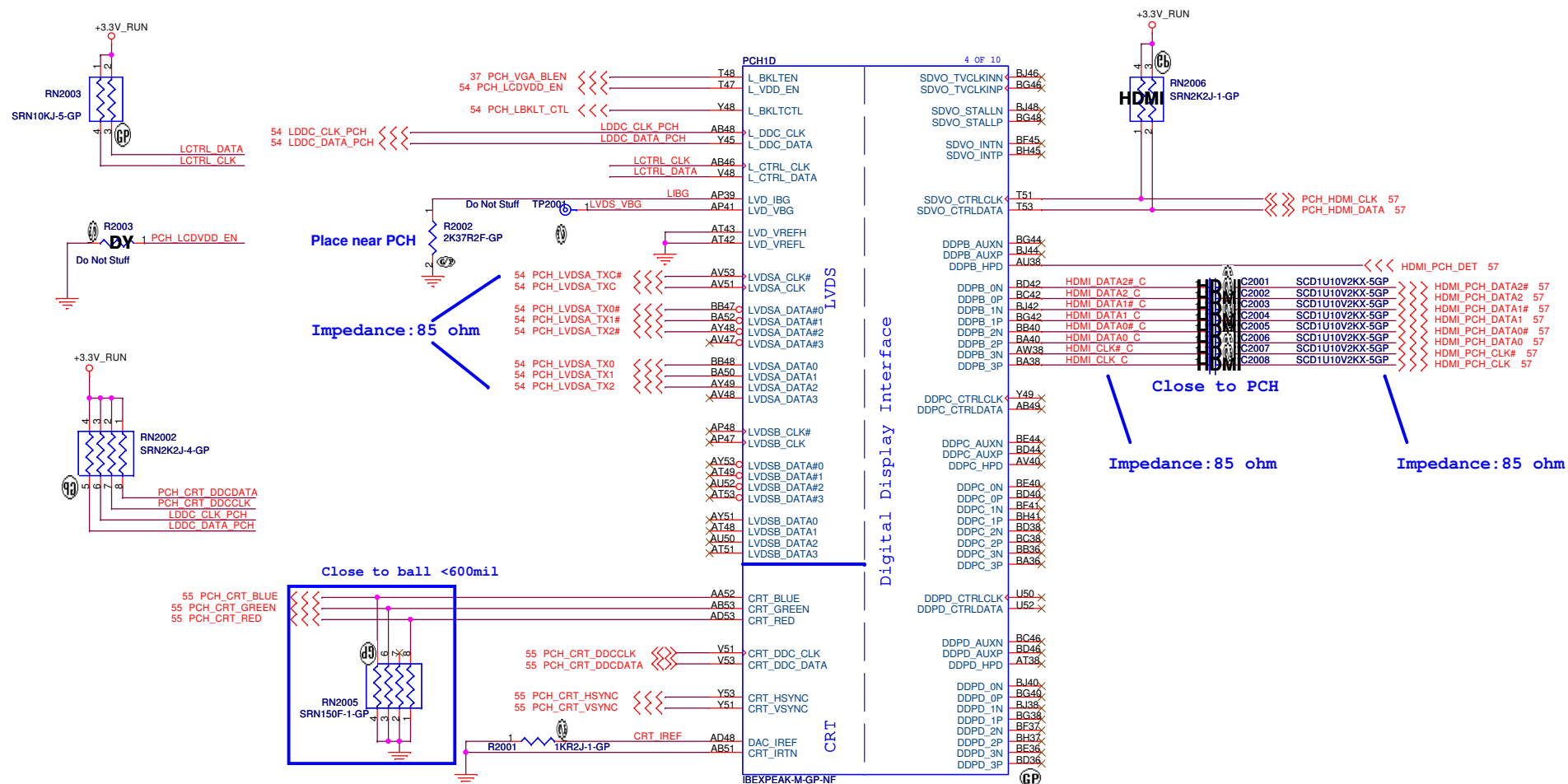


**Layout Note:**  
Place these C  
SO-DIMMB.

**Note:**  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

SSID = PCH



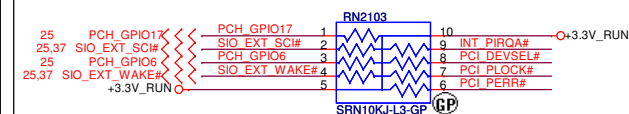
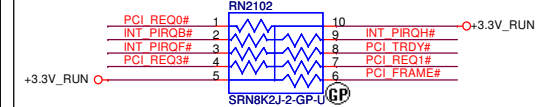
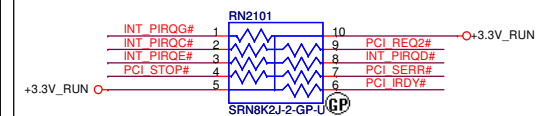
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Title			PCH (LVDS/CRT/DDI)	
Size	Document Number		Rev	
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**SSID = PCH**

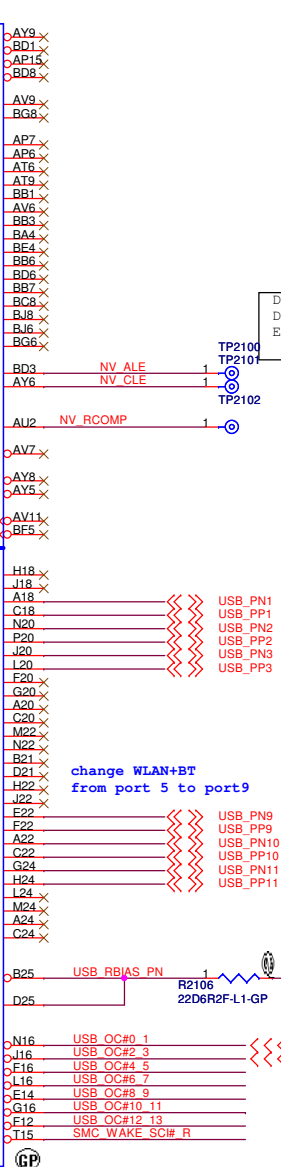
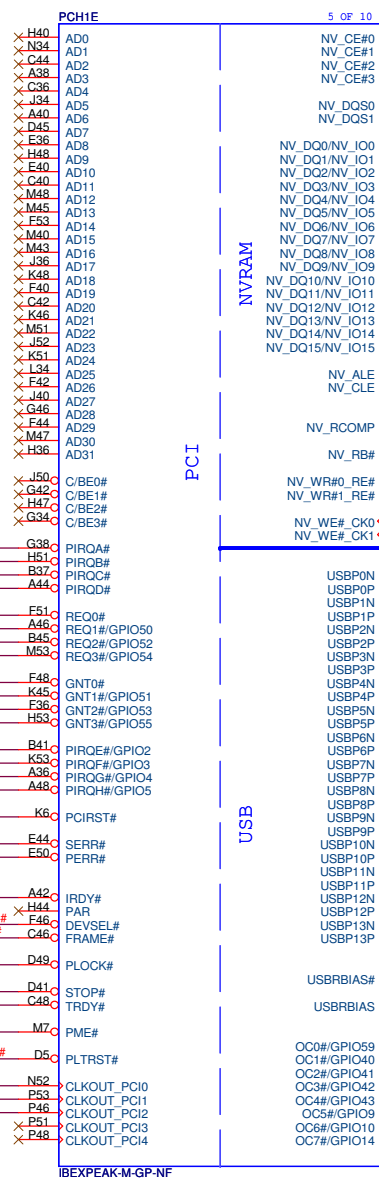
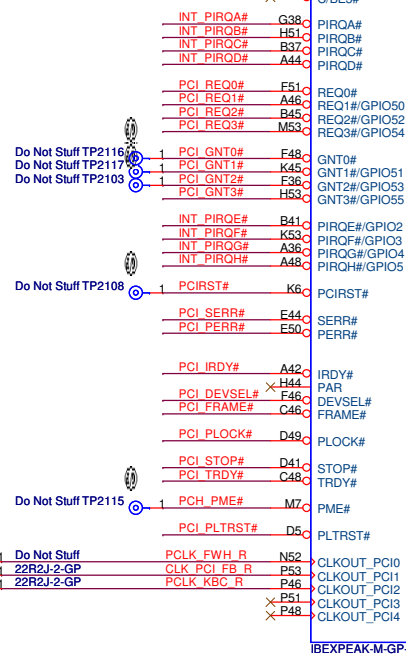
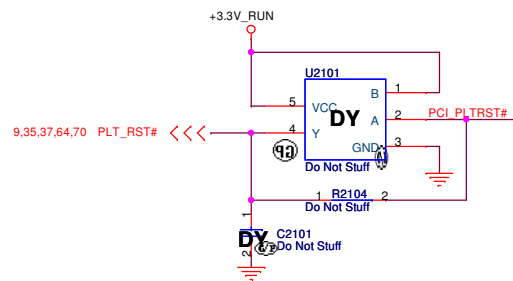
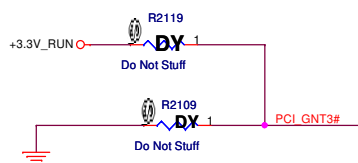


BOOT BIOS Strap

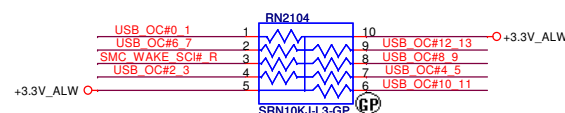
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block  
Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
-----------	---



USB	
Pair	Device
0	X
1	USB1 (Debug Port)
2	USB2 (Ext I/O BD)
3	USB3 (Ext I/O BD)
4	X
5	X
6	X
7	X
8	X
9	WLAN + Bluetooth
10	CARD READER
11	CAMERA
12	X
13	X



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**PCH (PCI/USB/NVRAM)**

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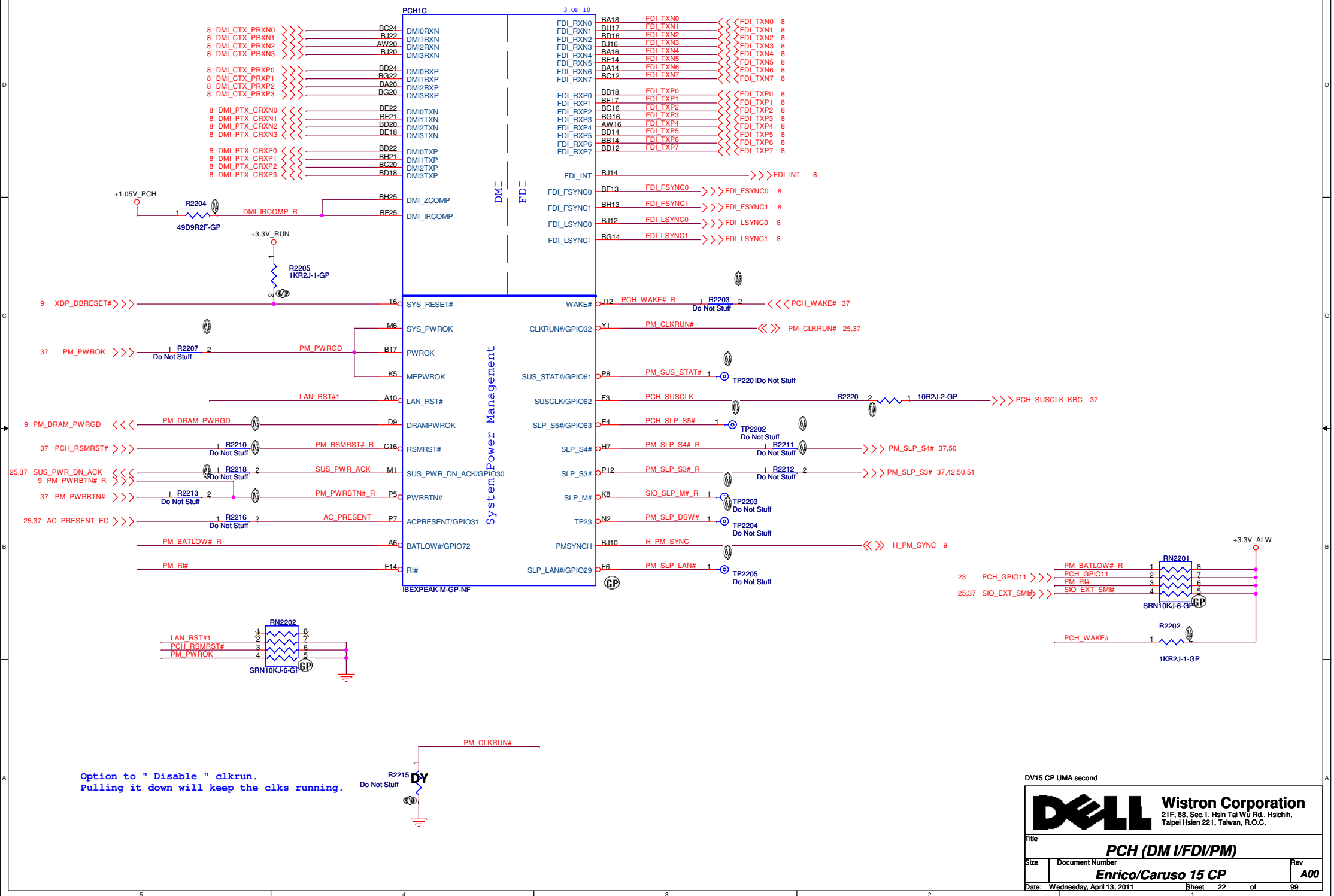
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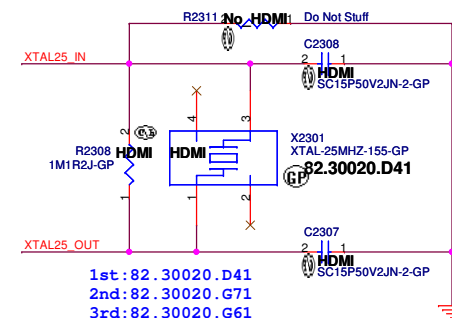
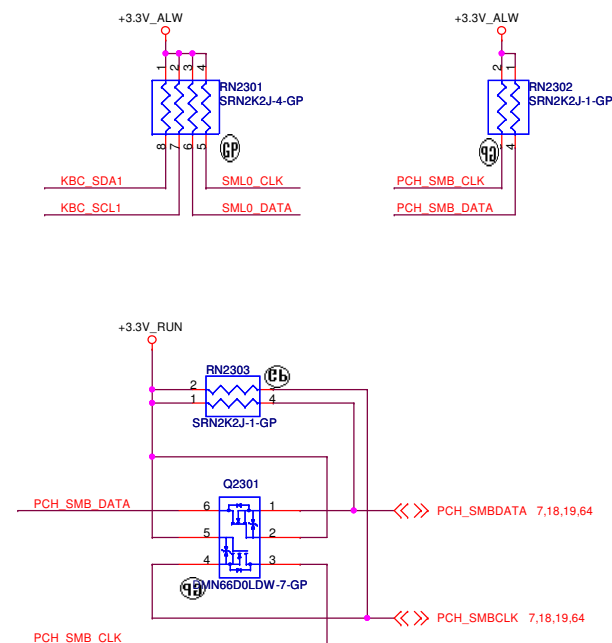
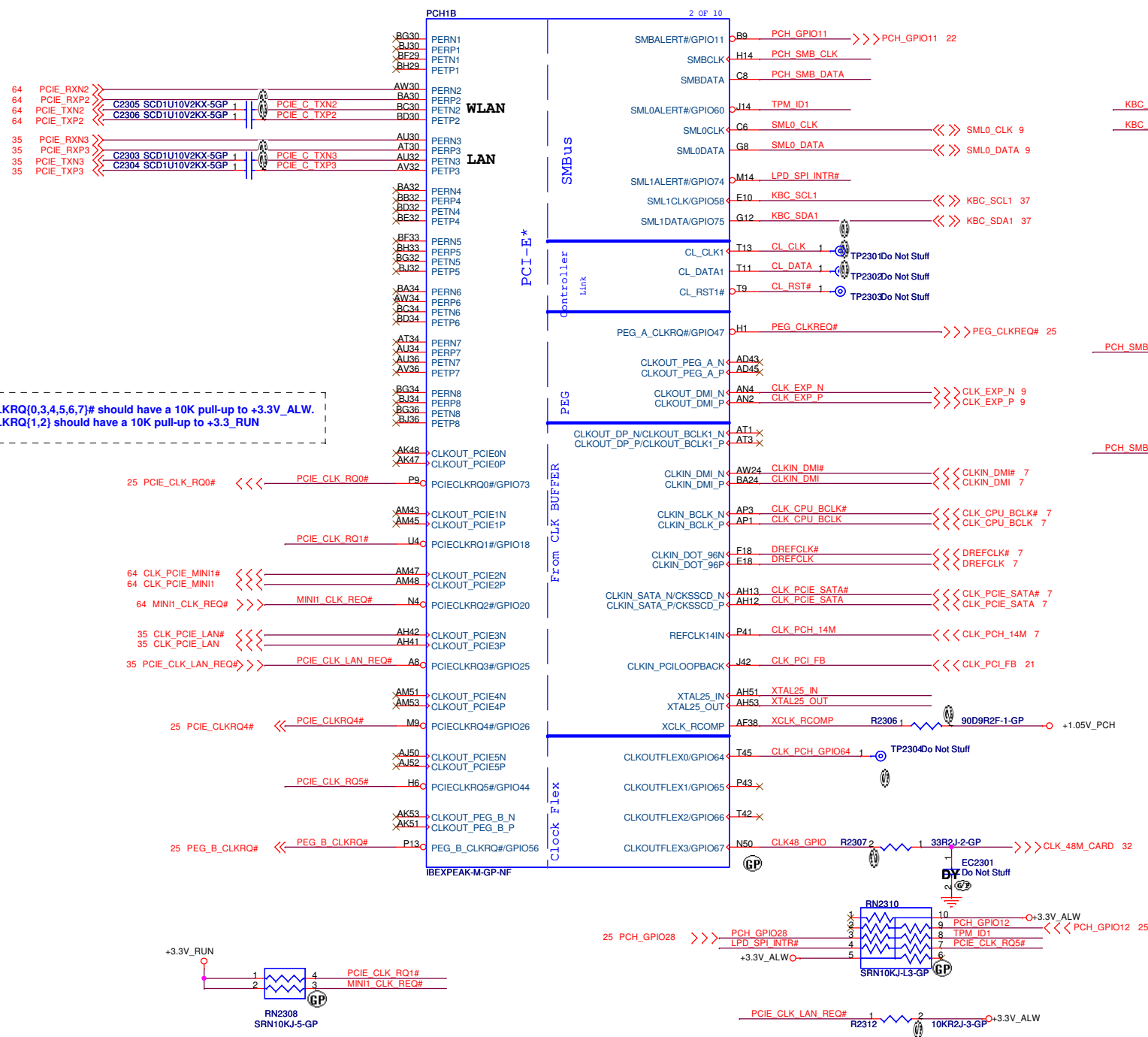
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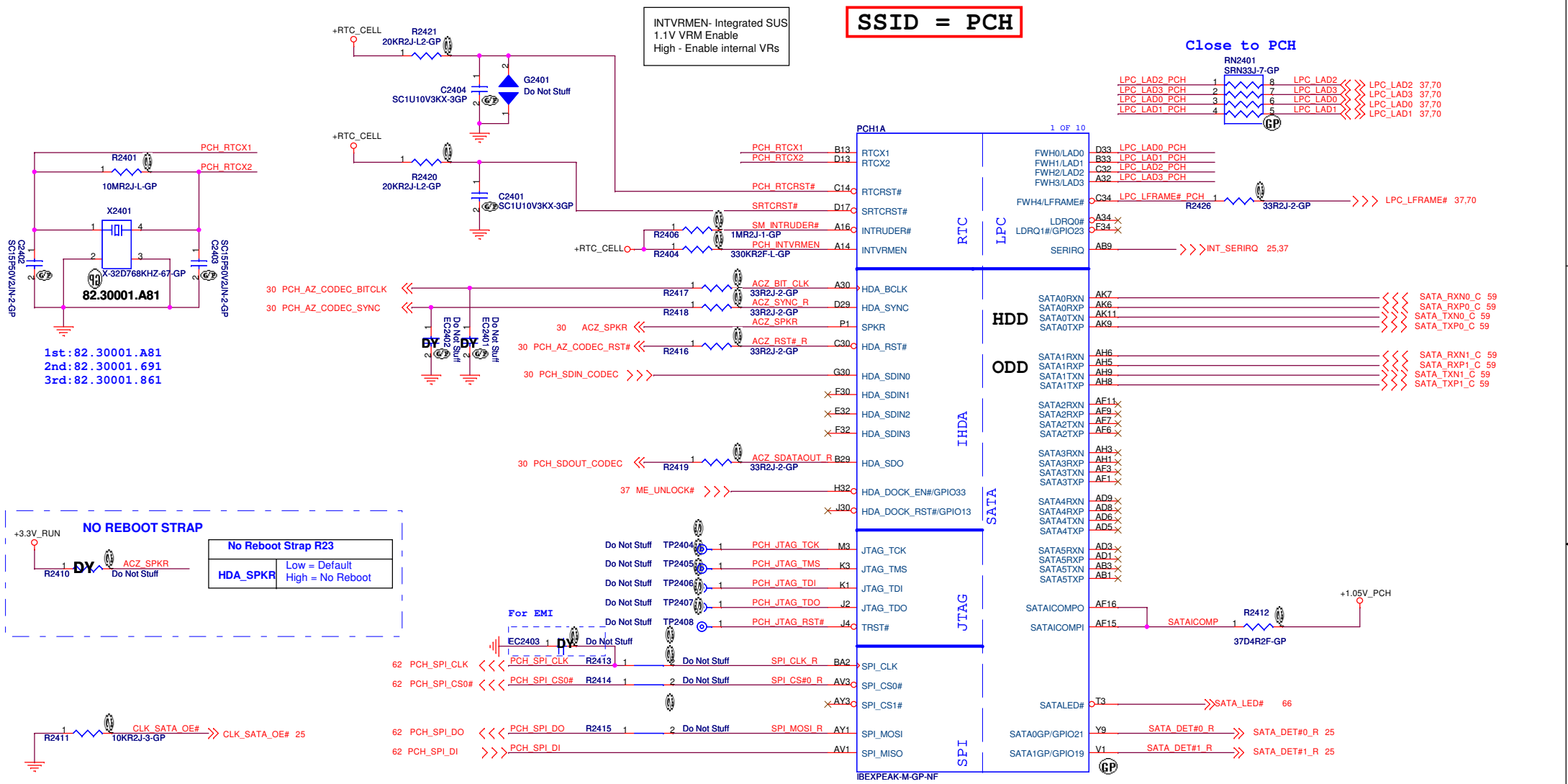
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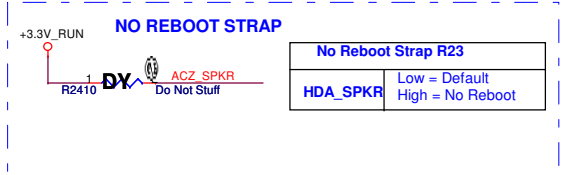
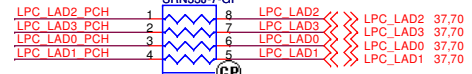
**SSID = PCH**





SSID = PCH

Close to PCH



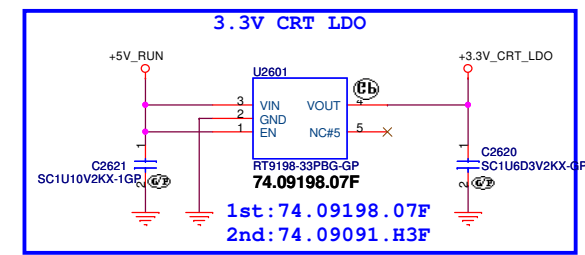
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Title <b>PCH (SPI/RTC/LPC/SATA/IHDA)</b>			
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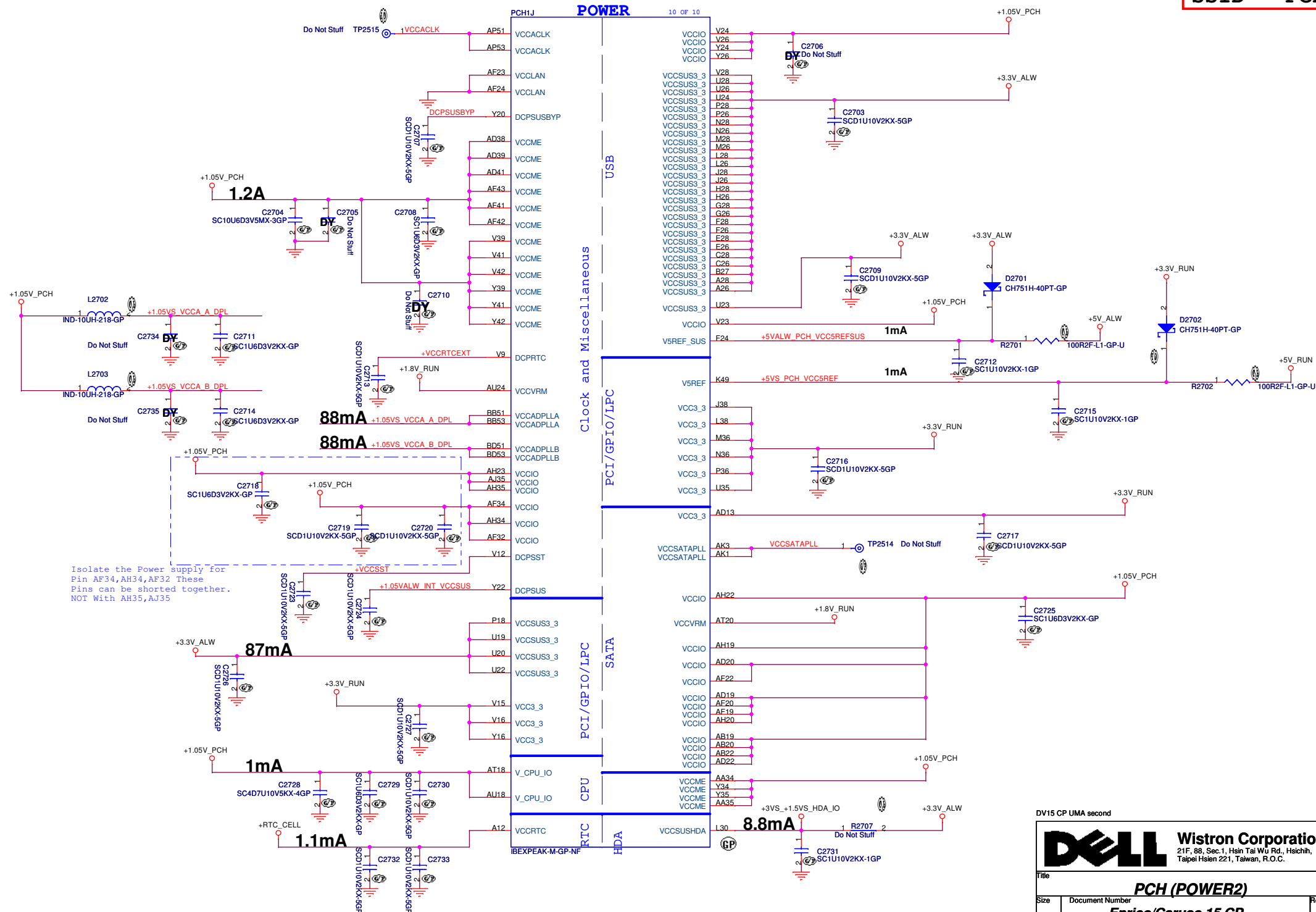


**SSID = PCH**



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Title			
<b>PCH (POWER1)</b>			
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**SSID = PCH**



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**PCH (POWER2)**

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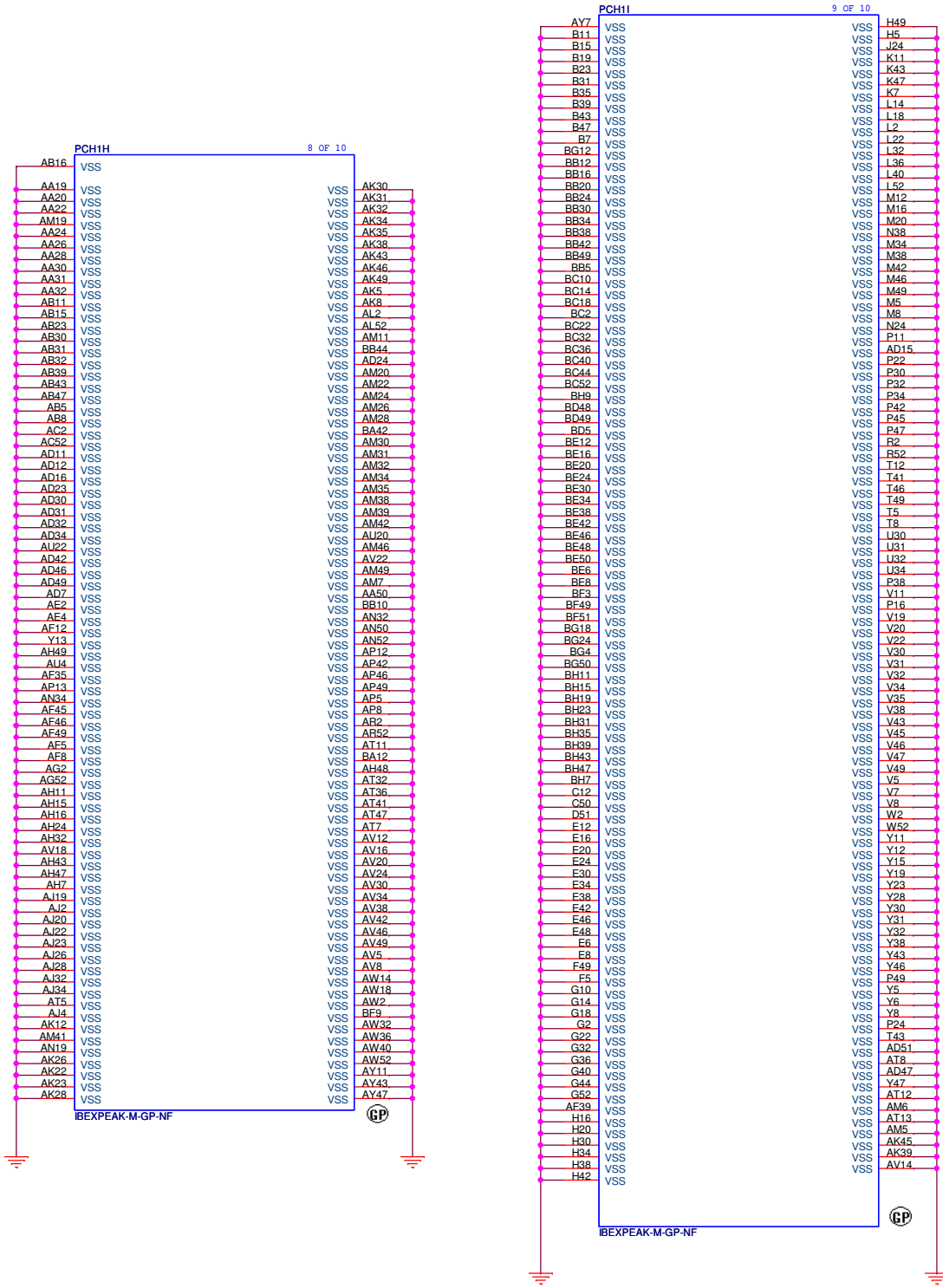
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1

SSID = PCH



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**DELL**

Title: **PCH (VSS)**

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Document Number  
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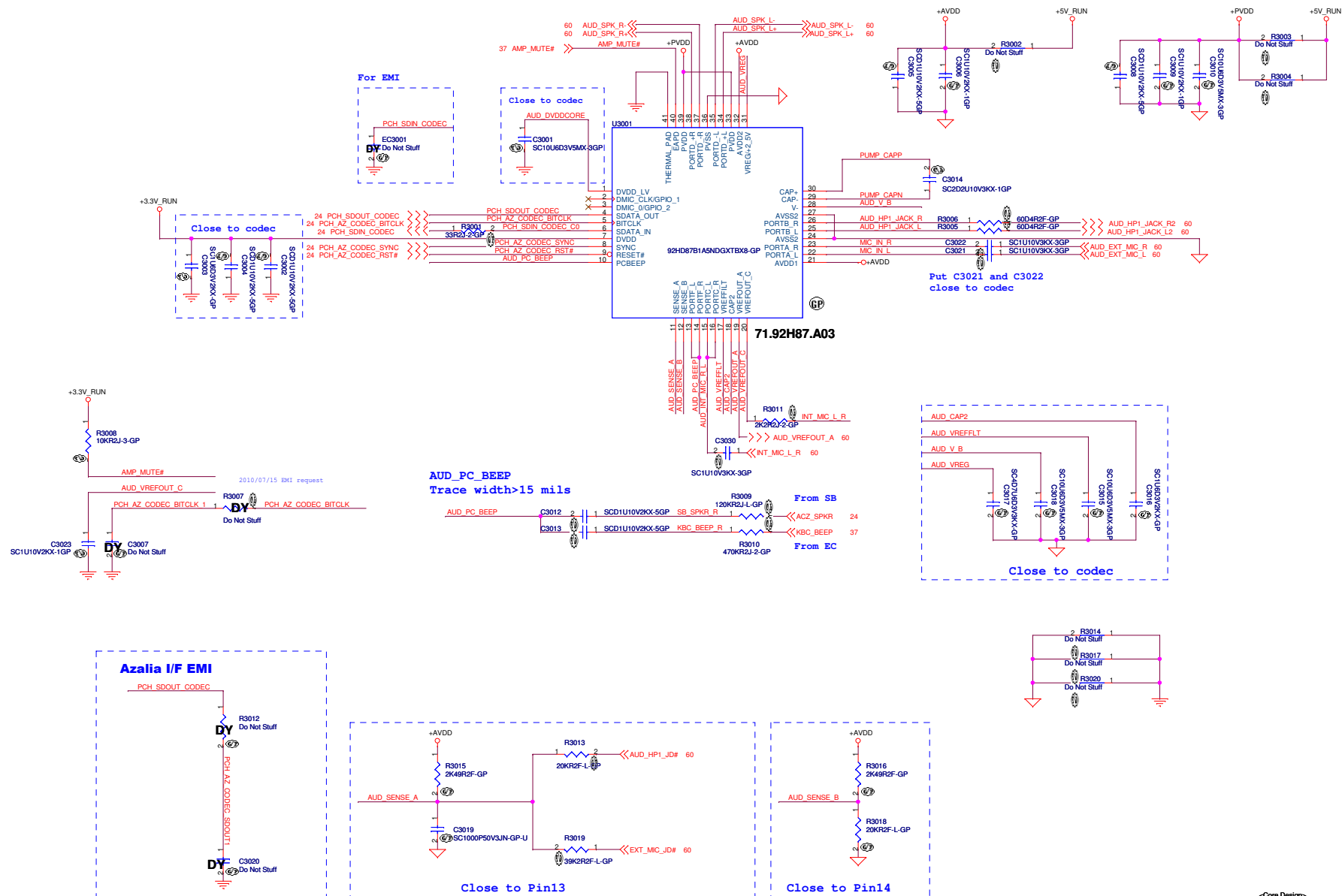
Date: Friday, April 08, 2011

**Reserved**

Rev  
**A00**


Sheet 29 of 99

SSID = AUDIO



(Blanking)

DV15 CP UMA second



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Title

Size  
A3

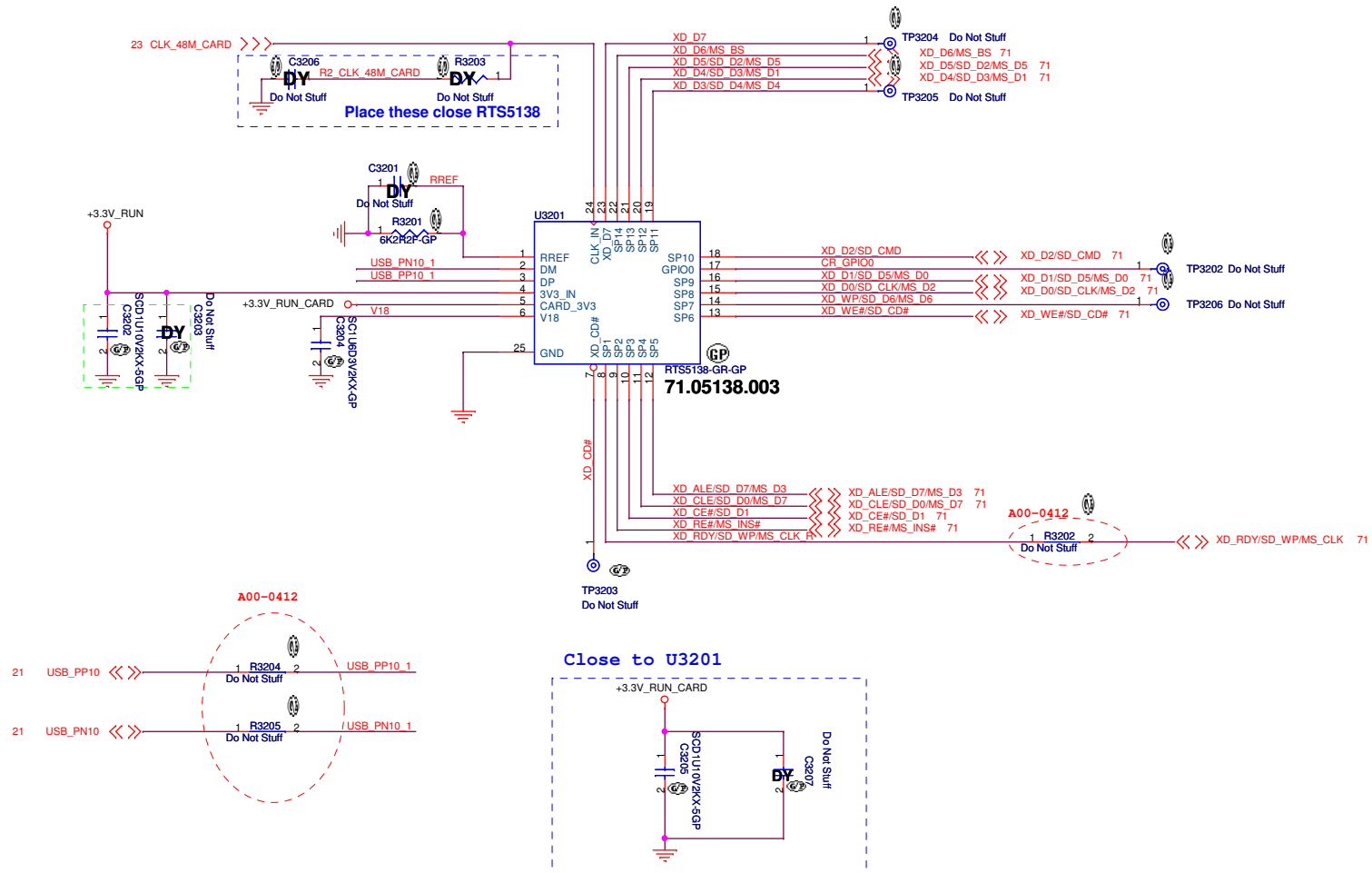
Document Number  
**Enrico/Caruso 15 CP**

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**A00**

Date: Friday, April 08, 2011

Sheet 31 of 99

SSID = SDIO



DV15 CP UMA second



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### **Card Reader-RTS5138**

Size	1
Custom	

Document Number **Enri****Enrico/Caruso 15 CP**

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## (Blanking)

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Title

**Reserved**

Size  
A3

Document Number
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Rev  
**A00****Enrico/Caruso 15 CP**

Date: Friday, April 08, 2011

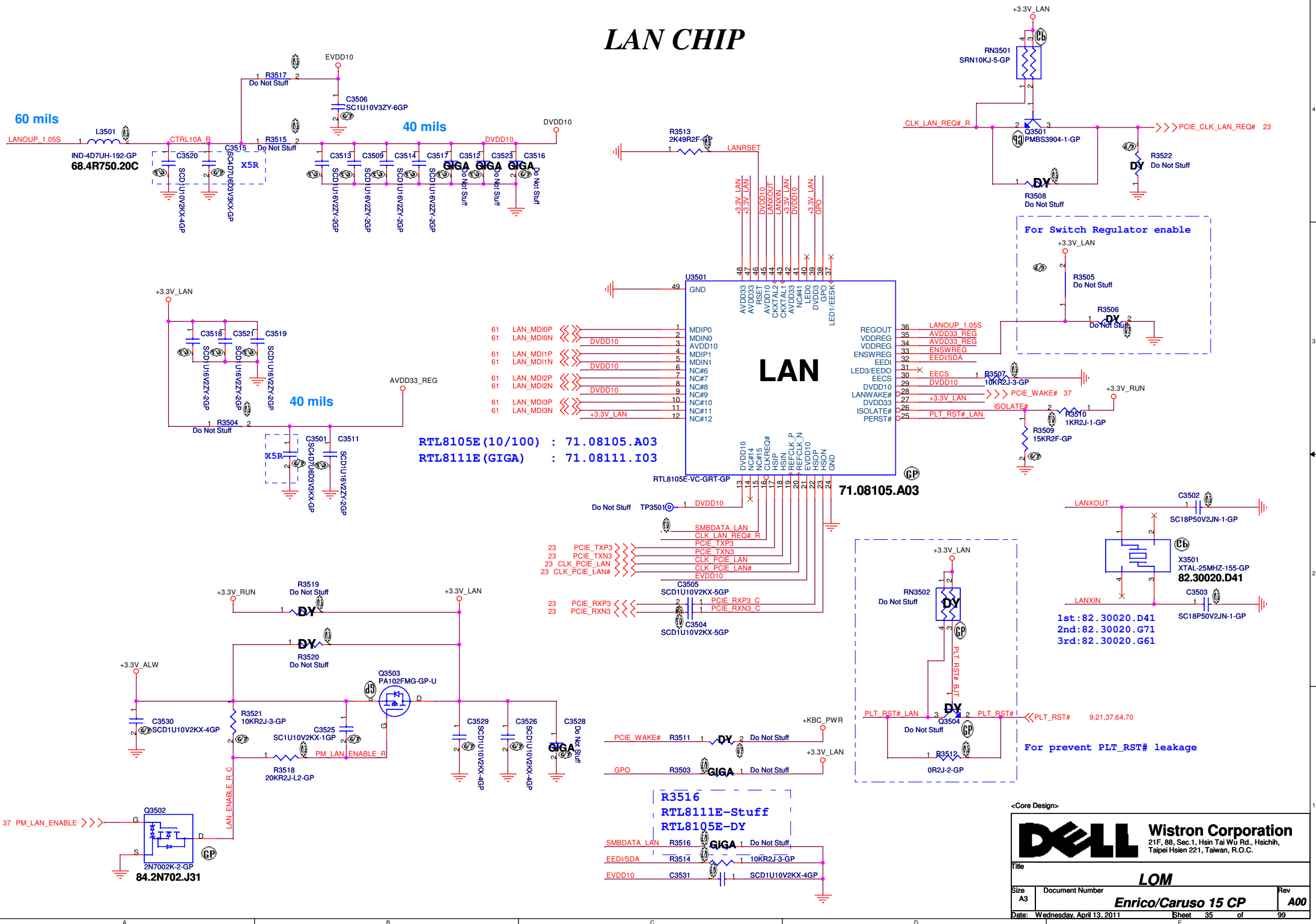
Sheet	33	of	99
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(Blanking)

DV15 CP UMA second

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Title <b><i>Reserved</i></b>			
Size A3	Document Number <b><i>Enrico/Caruso 15 CP</i></b>		Rev <b>A00</b>
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## LAN CHIP



## (Blanking)

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	Title
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**Reserved**

Size  
A3

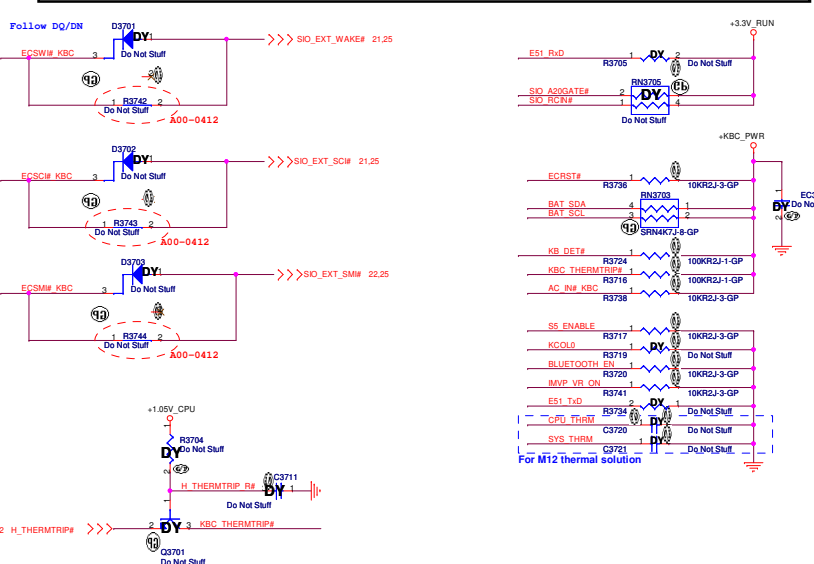
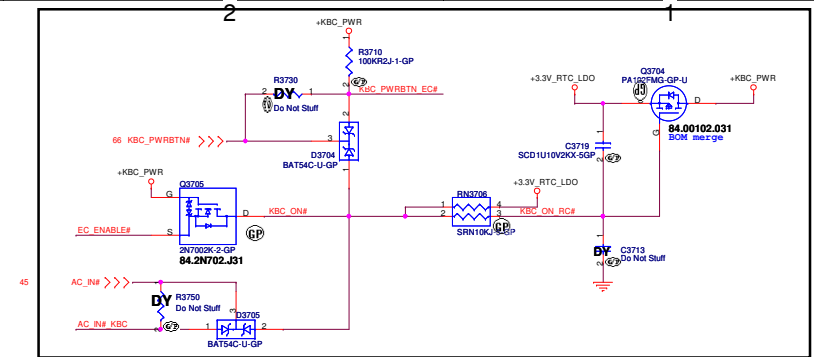
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Rev  
**A00**

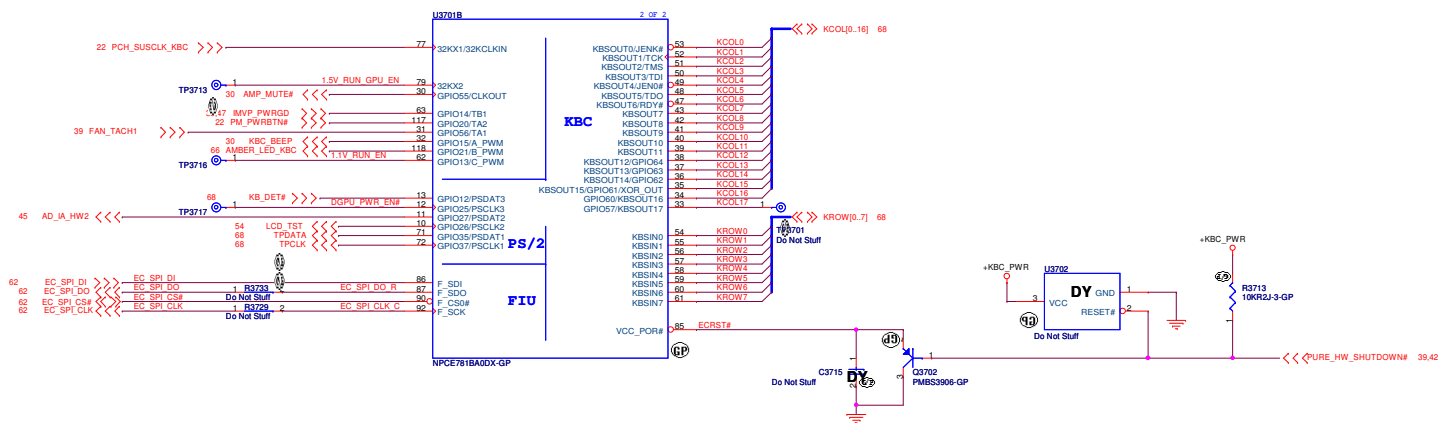
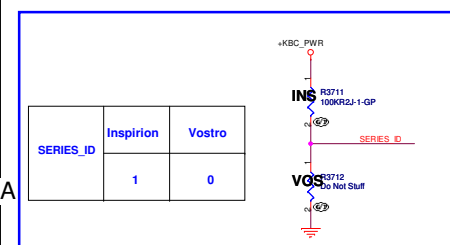
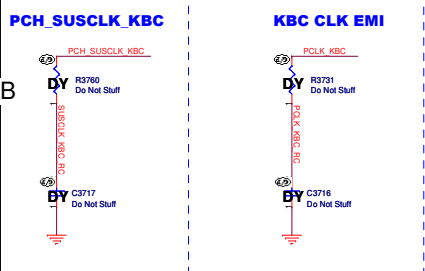
**Enrico/Caruso 15 CP**

Date: Friday, April 08, 2011

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EC HW Strap Pin			
Net Name	Pin	GPIO	Note
BLUETOOTH_EN	83	GP076	Pull-Low
USB_PWR_EN#	110	GP082	Don't Pull-Low
E51_TXD	111	GP083	Don't Pull-Low
AC_PRESENT_EC	112	GP084	Don't Pull-Low
KCOL0	53	KBS0U70	Don't Pull-Low
KCOL4	49	KBS0U74	Don't Pull-Low
KCOL9	41	KBS0U79	Don't Pull-Low



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Size  
A3

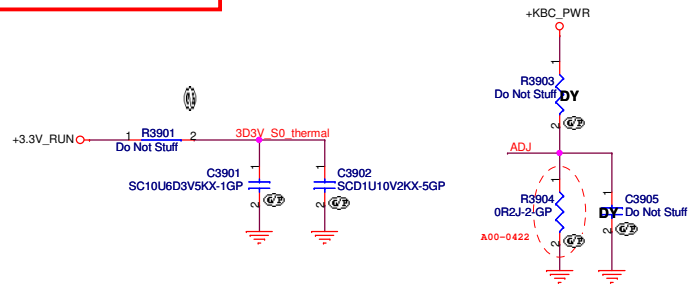
Document Number  
Enrico/Caruso 15 CP

Date: Friday, April 08, 2011

Rev  
A00

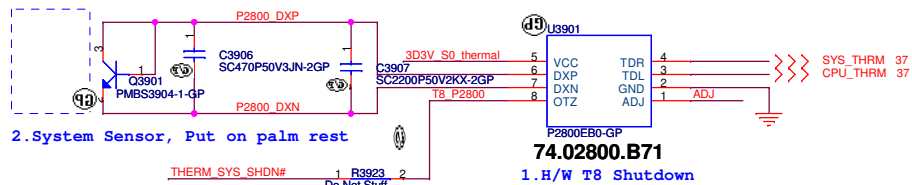
Sheet 38 of 99

SSID = Thermal



Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.

Remove R3908 and  
put C3906 close to Q3901

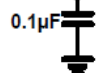
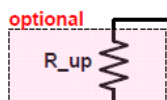


2. System Sensor, Put on palm rest

THERM\_SYS\_SHDN#

## Thermal sensor P2800

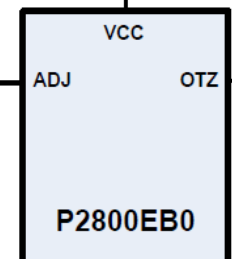
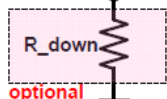
3.0V to 3.6V



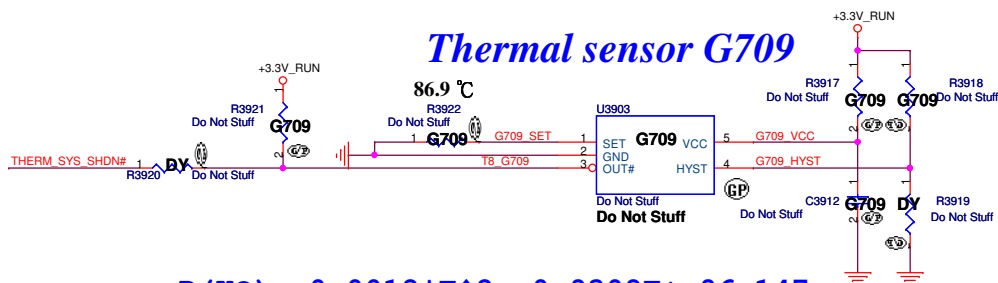
Option 1: OTZ=95°C → ADJ=3.3V

Option 2: OTZ=85°C → ADJ=Floating

Option 3: OTZ=90°C → ADJ=GND

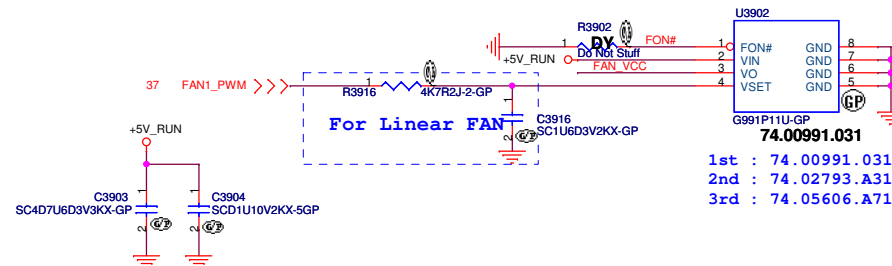


## Thermal sensor G709

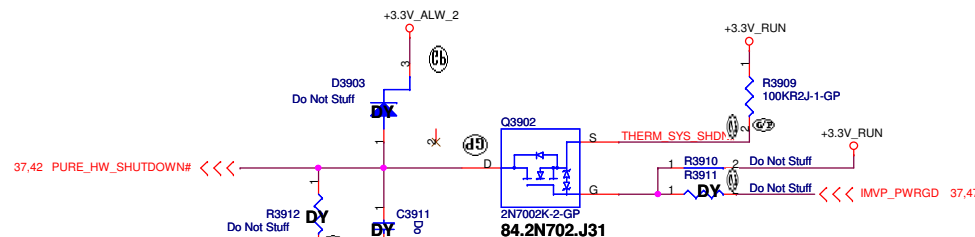
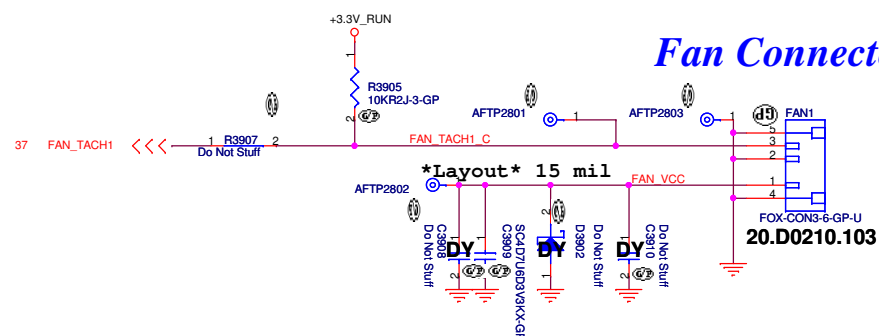


$$R(K\Omega) = 0.0012 * T^2 - 0.9308T + 96.147$$

## Fan controller




## Fan Connector



DV15 CP UMA second

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Title			
<b>Reserved</b>			
Size A3	Document Number <b>Enrico/Caruso 15 CP</b>		Rev <b>A00</b>
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Size  
A3

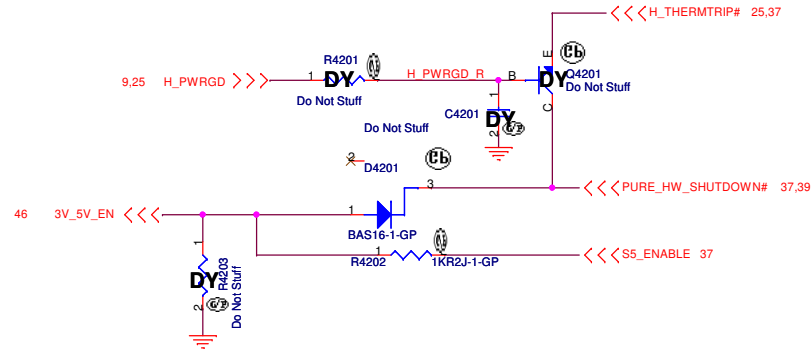
Document Number  
**Enrico/Caruso 15 CP**

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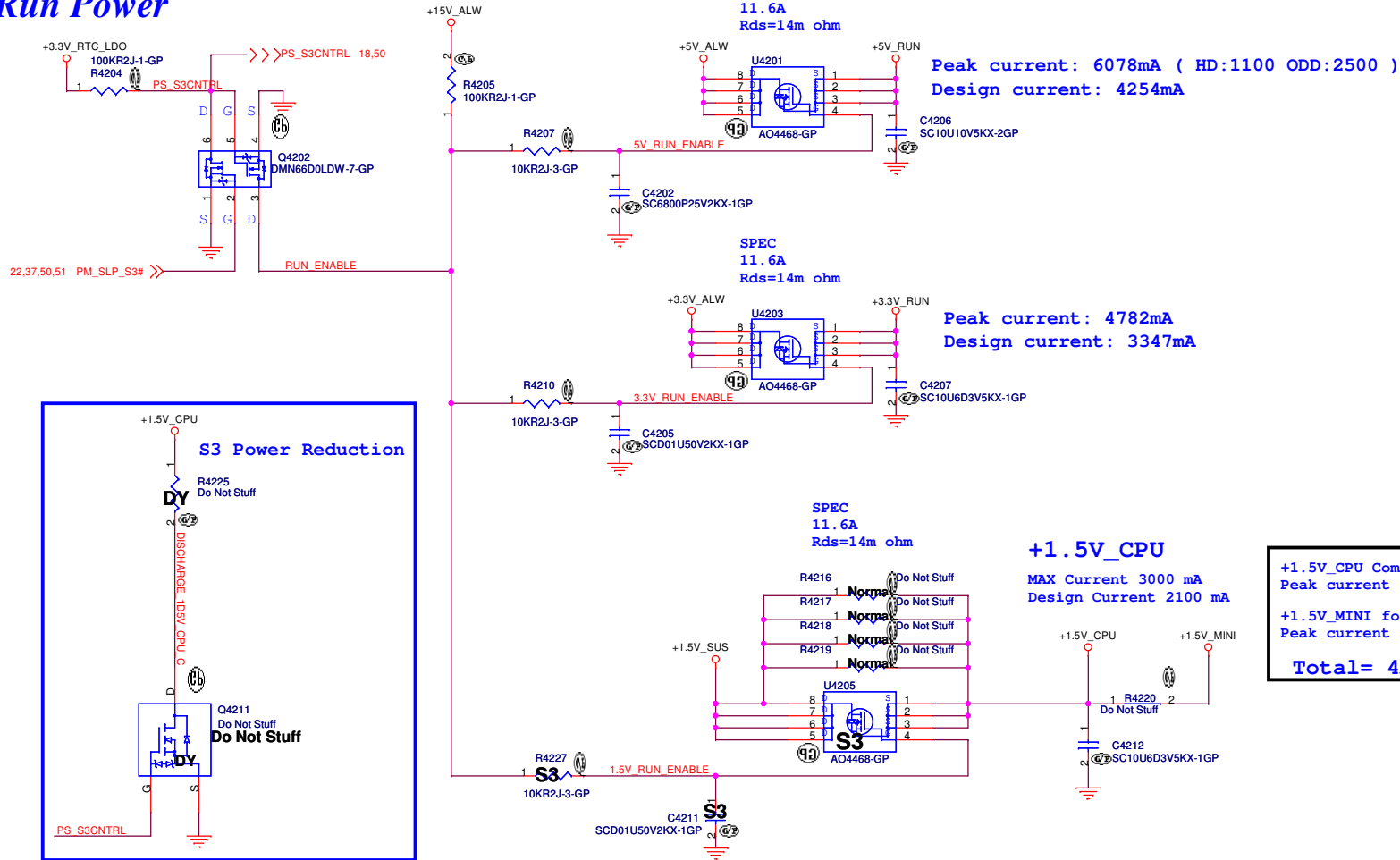
Date: Friday, April 08, 2011

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**SSID = Reset.Suspend**



## Run Power



DV15 CP UMA second



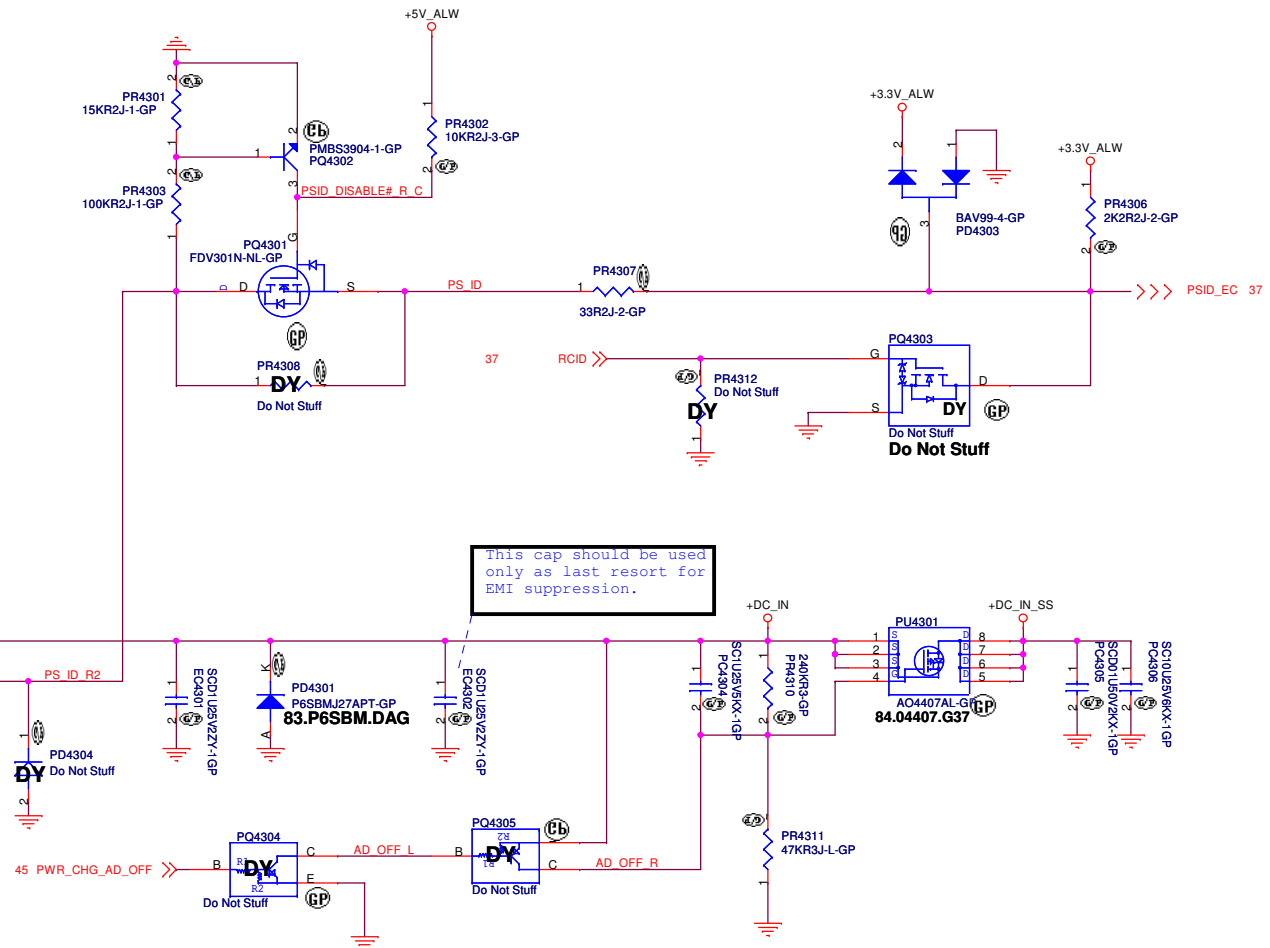
Power Plane Enable		
Size A3	Document Number	Rev
Enrico/Caruso 15 CP		A00
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SSID = PWR.Support

## DCin CONN

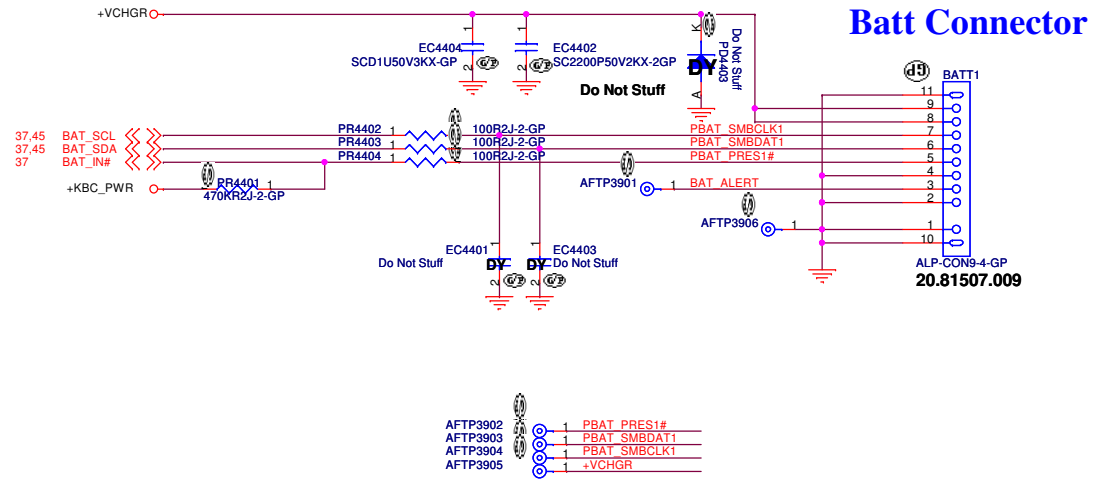
remove EL4301 for  
current rating

Follow DW50

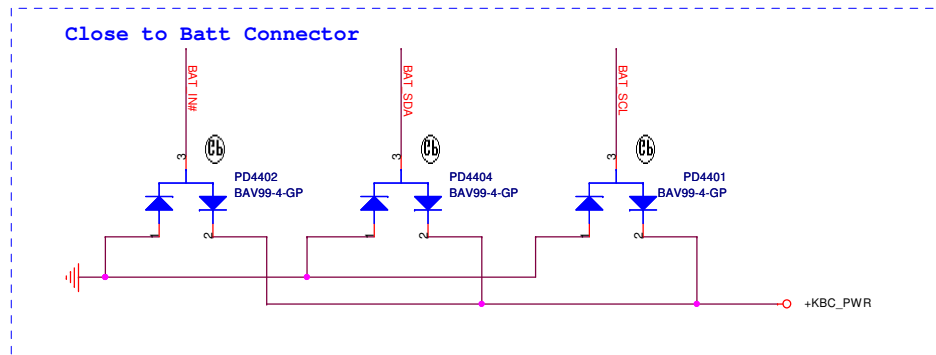


DV14 CP

SSID = BATT CONN



For actual location, need to be swap all pin



### <Core Design>



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Title

**BATT CONN**

Size  
A3

Document Number
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**Enrico/Caruso 15 CP**

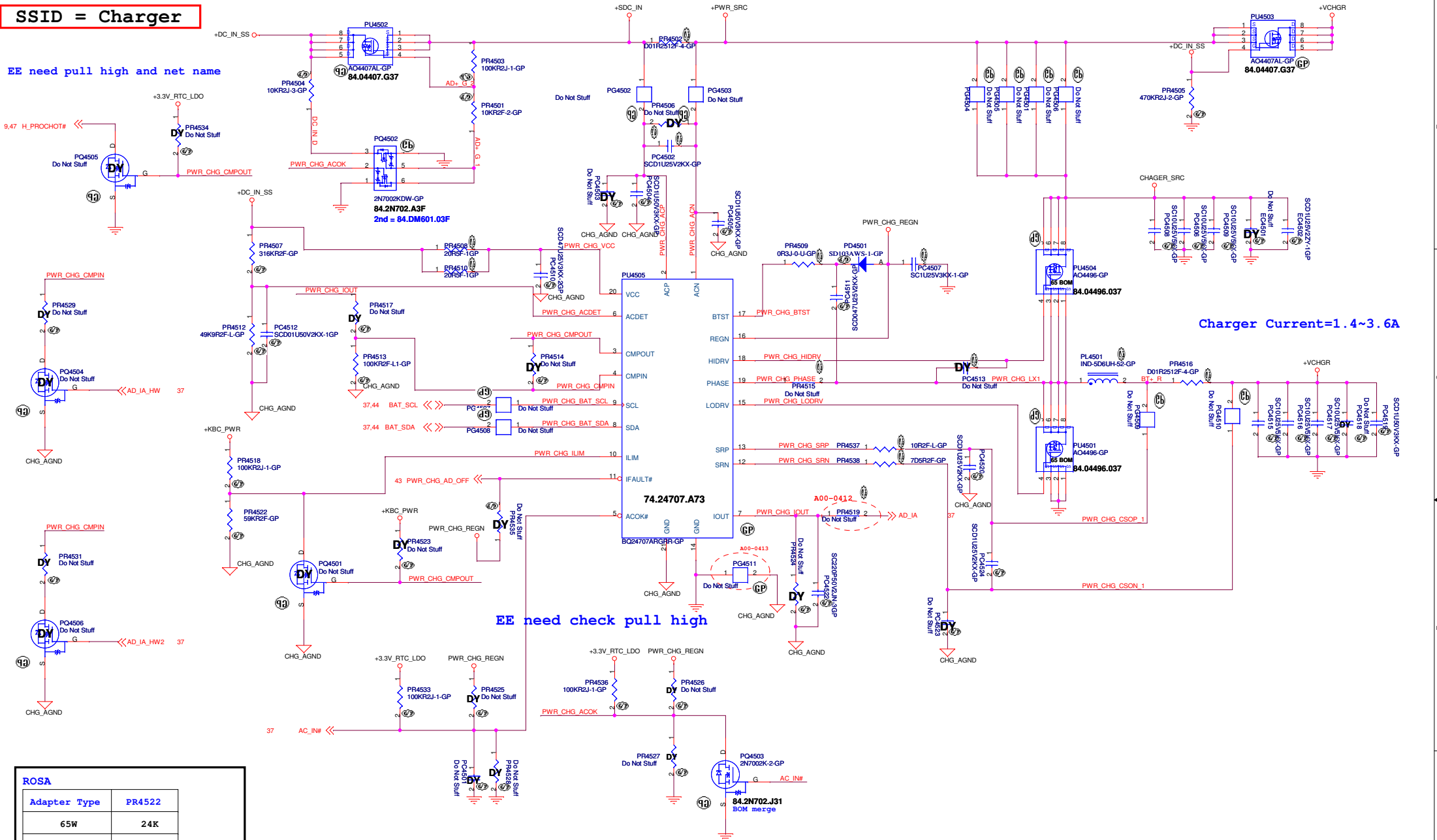
Rev  
**A00**

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SSID = Charger

EE need pull high and net name



EE need check pull high

Charger Current=1.4~3.6A

Adapter Type	PR4522
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

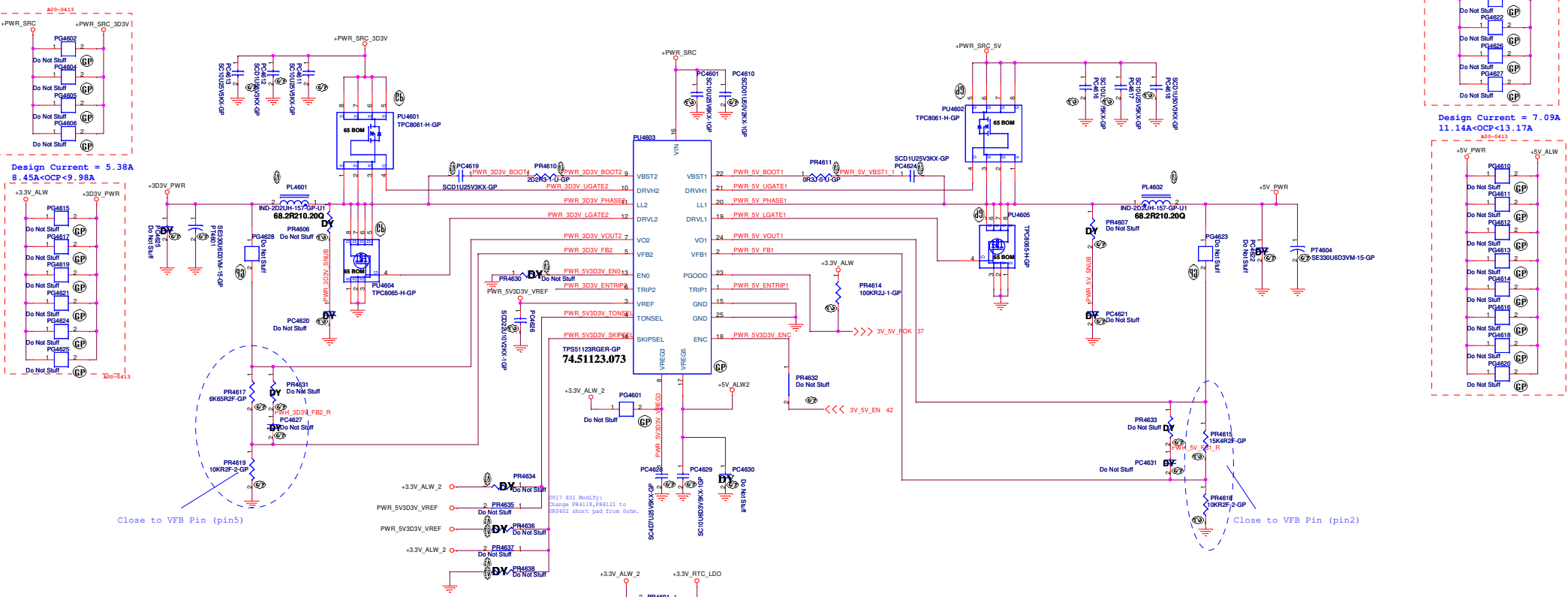
<Core Design>



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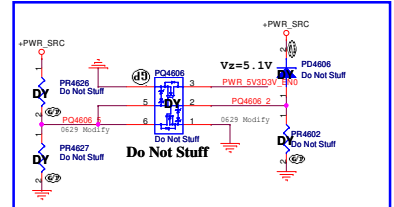
Title			
<b>CHARGER BQ24707</b>			
Size	Document Number	Rev	
Custom	<b>Enrico/Caruso 15 CP</b>	<b>A00</b>	
Date:	Friday, April 15, 2011	Sheet 45 of	99

SSID = PWR.Plane.Regulator\_5v3p3v



Design Current = 5.38A  
8.45A < OCP < 9.98A

Design Current = 7.09A  
11.14A < OCP < 13.17A

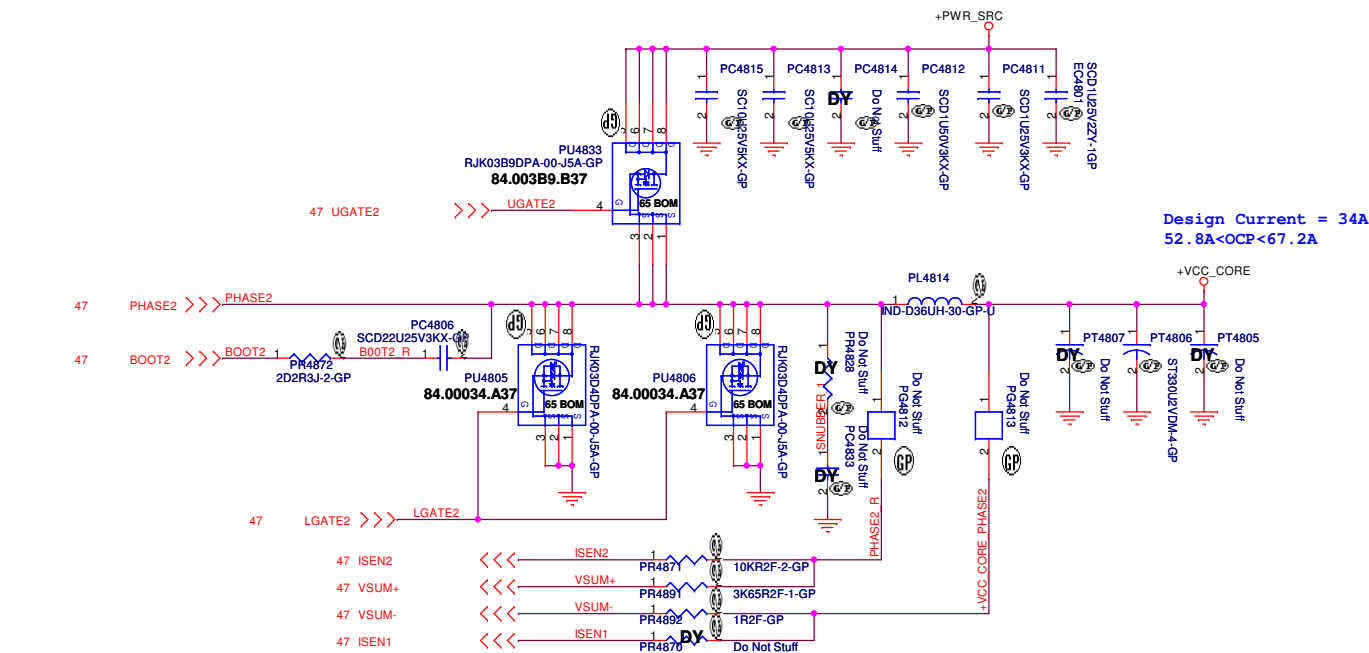


TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 2.2U PCMC063T-2R2MH Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20Q  
O/P cap: 330U 6.3V SE330U6D3VM-15-GP 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L  
O/P cap: 330U 6.3V SE330U6D3VM-15-GP 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L  
H/S: TPC8061-H / 21mohm/30mOhm4.5Vgs/ 84.08061.037  
L/S: TPC8065-H / 12mohm/15mOhm4.5Vgs/ 84.08065.037



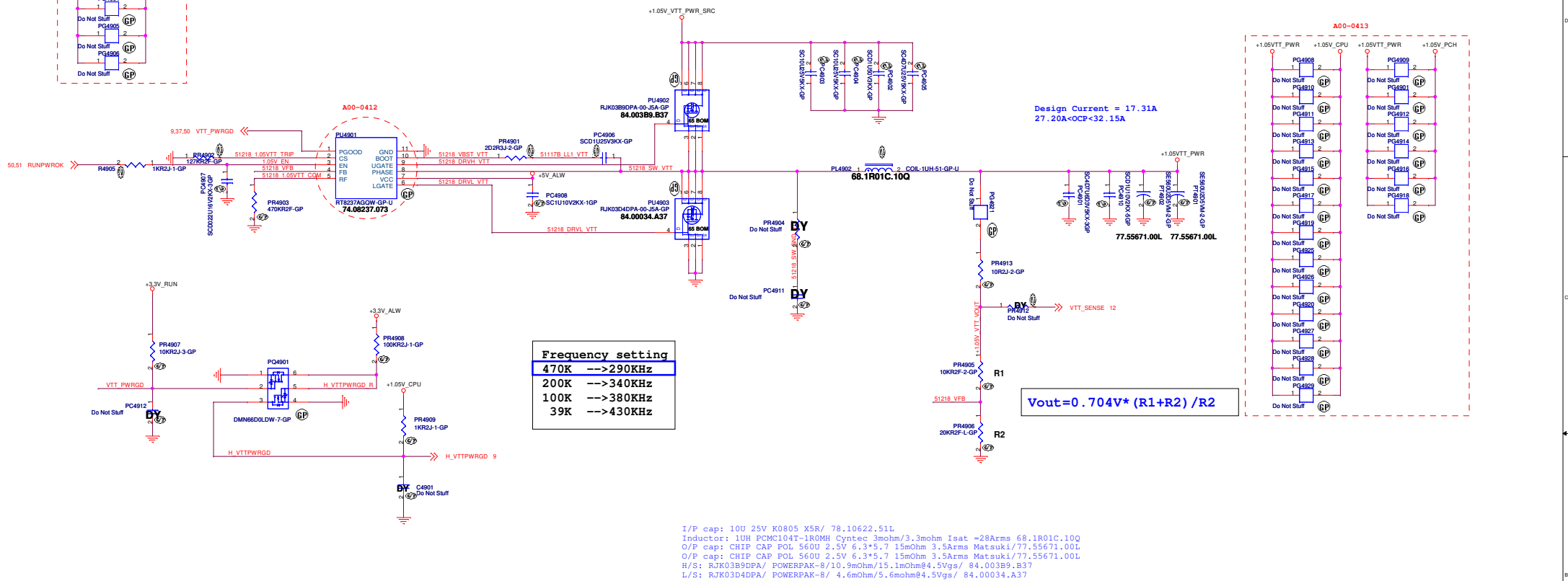


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.36UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C  
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L  
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37  
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

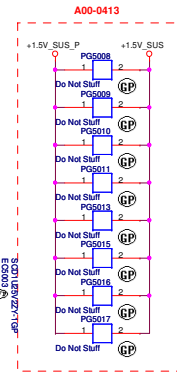
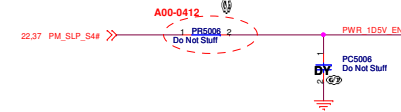
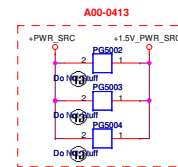
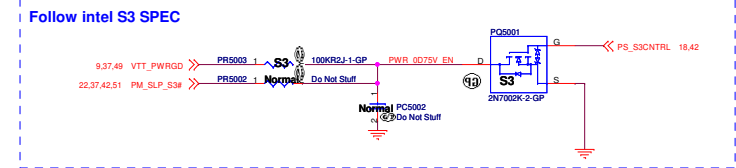
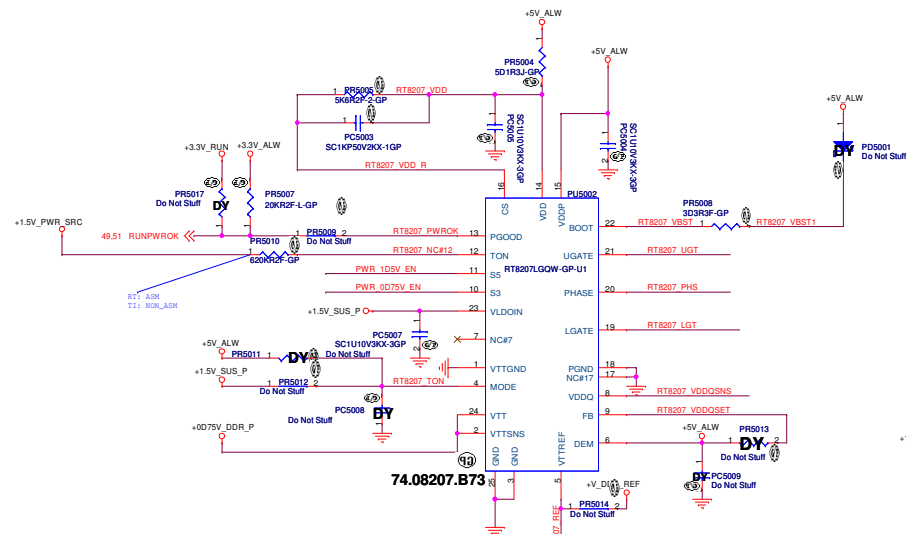
DV15 CP UMA second



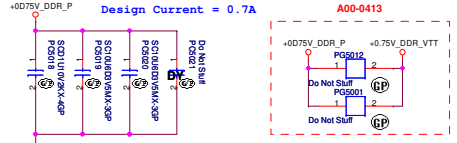
# RT8237A for +1.05V\_VTT



```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



Design Current = 7.35A  
11.55A<OCP<13.65A

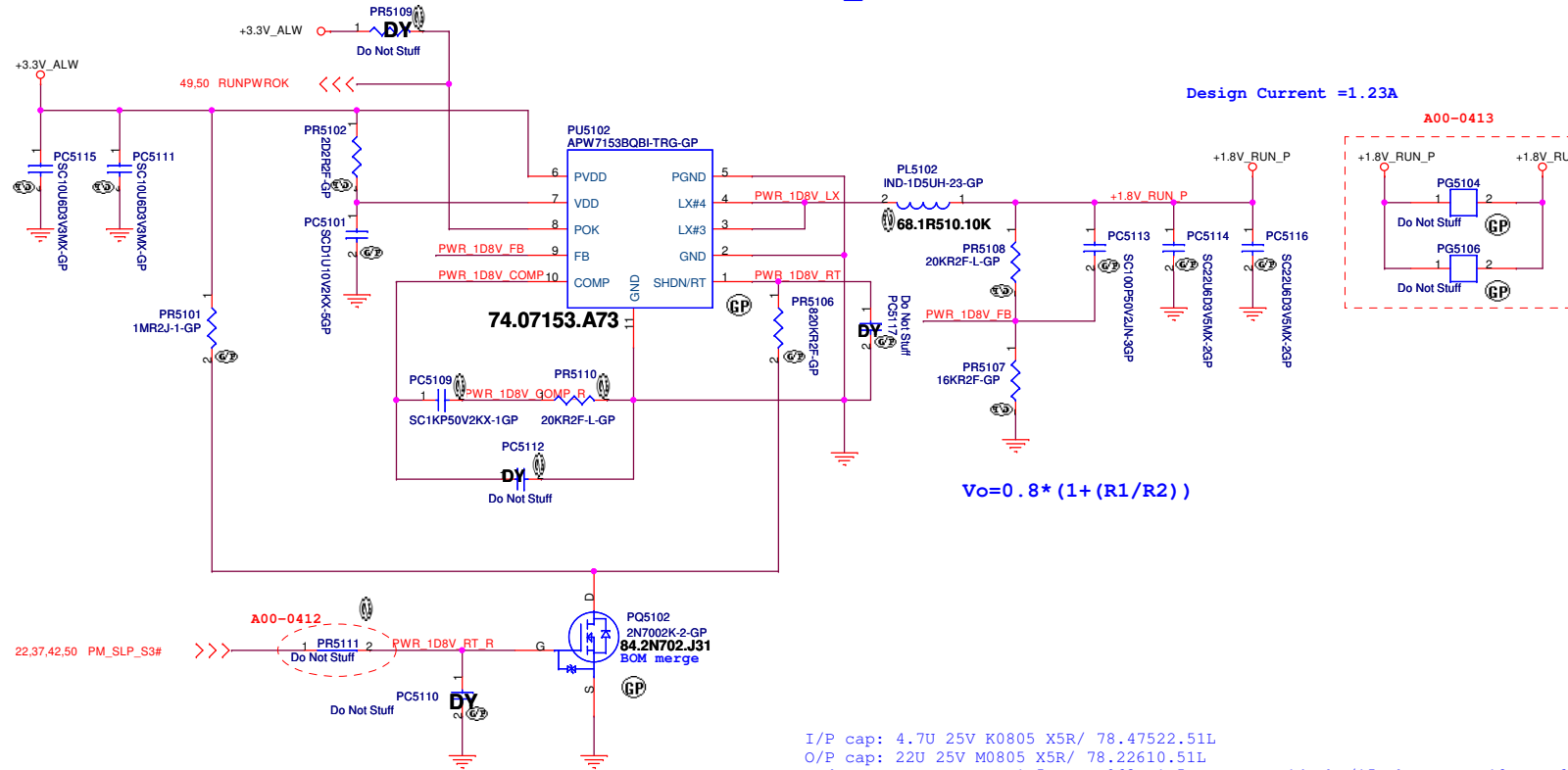


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K0405 X5R/ 78.10622.51L  
Inductor: 1.5U PCMC118T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10.  
O/P cap: CHIP CAP POL 560U 2.5V 6.3\*5.7 15mOhm 3.5Arms Matsuki/77.55671.00L  
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.0003B.B37  
L/S: RJK03B9DPA/ POWERPAK-8/ 4.6mOhm/5.6mOhm@4.5Vgs/ 84.0003A.A37

# APW7153B for 1D8V\_RUN



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L  
 O/P cap: 22U 25V M0805 X5R/ 78.22610.51L  
 Inductor: CHIP CHOKE 1.5U PCMC063T-1R5MN Cynotec 14mohm/15mohm Isat =18Arms 68.1R510.10K

INS 100 NONE SURGE

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Title			
<b><i>APW7153B for 1D8V RUN</i></b>			
Size	Document Number	Rev	
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<b><i>Enrico/Caruso 15 CP</i></b>			
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Title	Author	Date	Page	Page	Page	Page	Page	Page	Page

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A3

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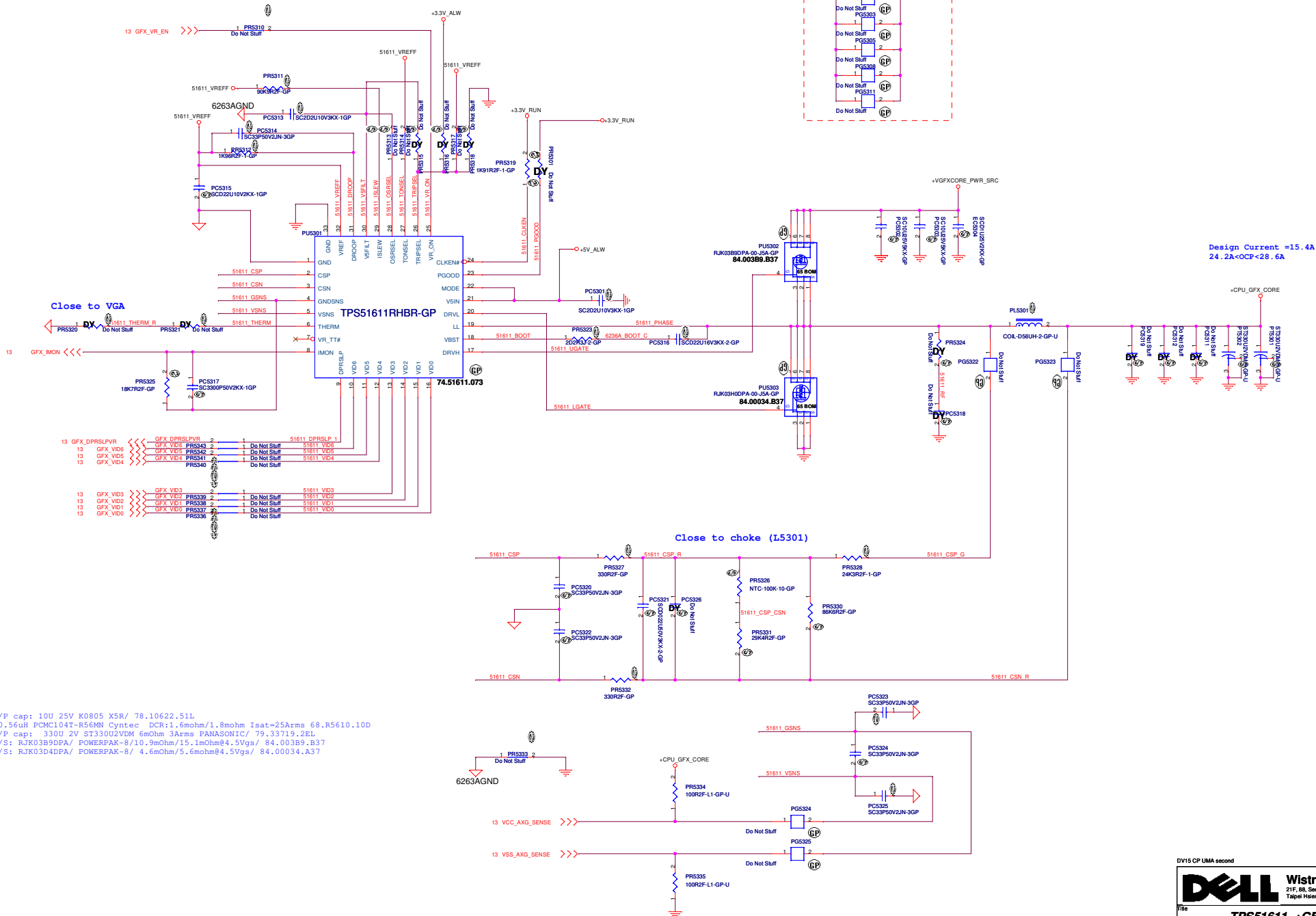
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**A00**

**Enrico/Caruso 15 CP**

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```
SSID = CPU.GFX.Regulator
```



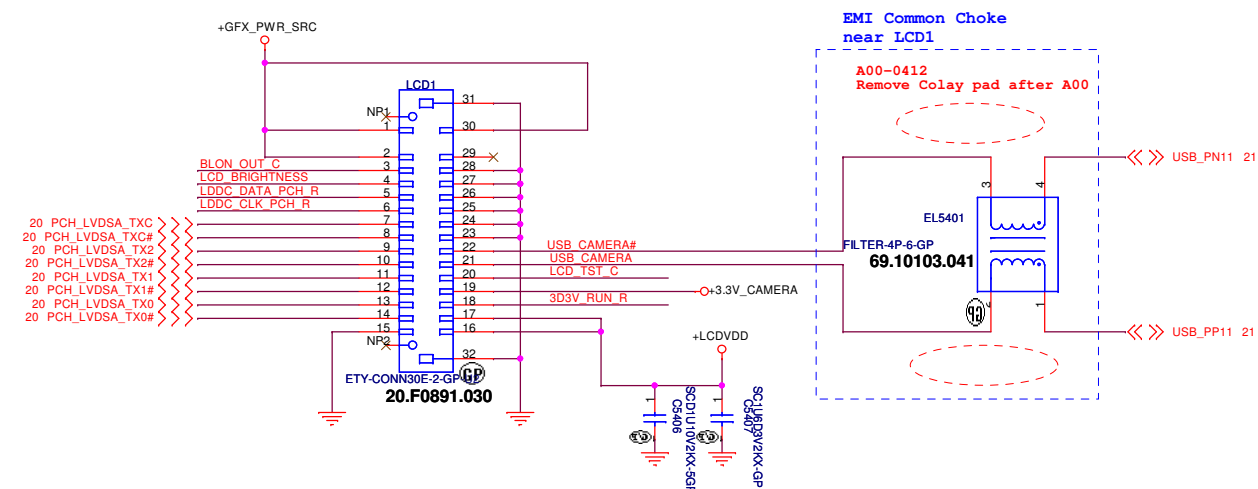
```

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
10.56uH PCCM104T-R56mN Cytdec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2V S1330U2V6M 6mohm 3Arms PANASONIC/ 79.33719.2EL
H/S: RJR03B9DPA/ POWERPAK-8/ 10.9mohm/1.51mohm4.5Vg/ 84.003B9.B37
L/S: RJR03D4DPA/ POWERPAK-8/ 4.6mohm/5.6mohm4.5Vg/ 84.00034.A37

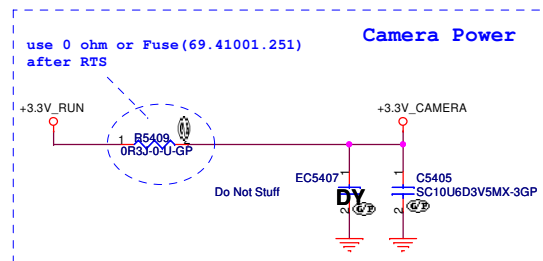
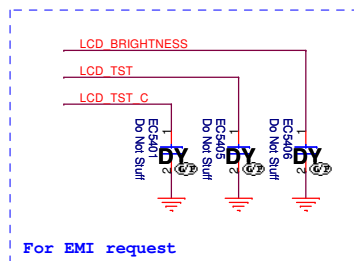
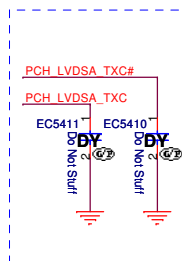
```

**SSID = VIDEO**

## LVDS CONNECTOR

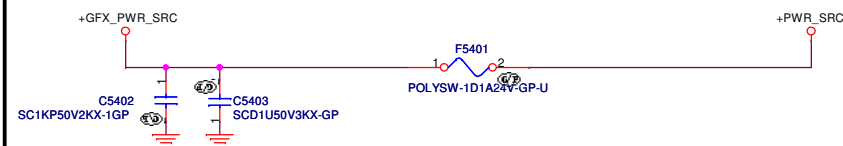


Close to LVDS connector



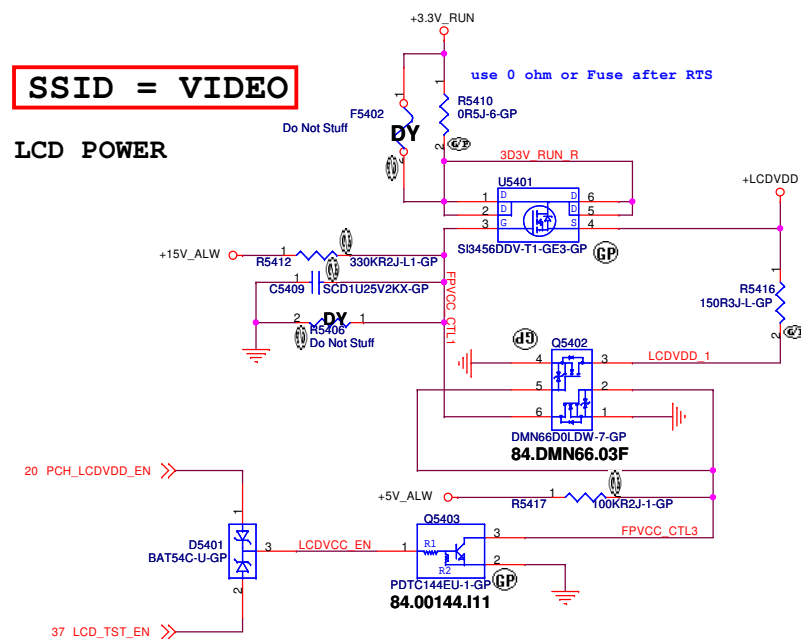
**SSID = Inverter**

## INVERTER POWER



**SSID = VIDEO**

## LCD POWER



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Title

### **LCD/Inverter Connector**

Size  
A3

Document Number

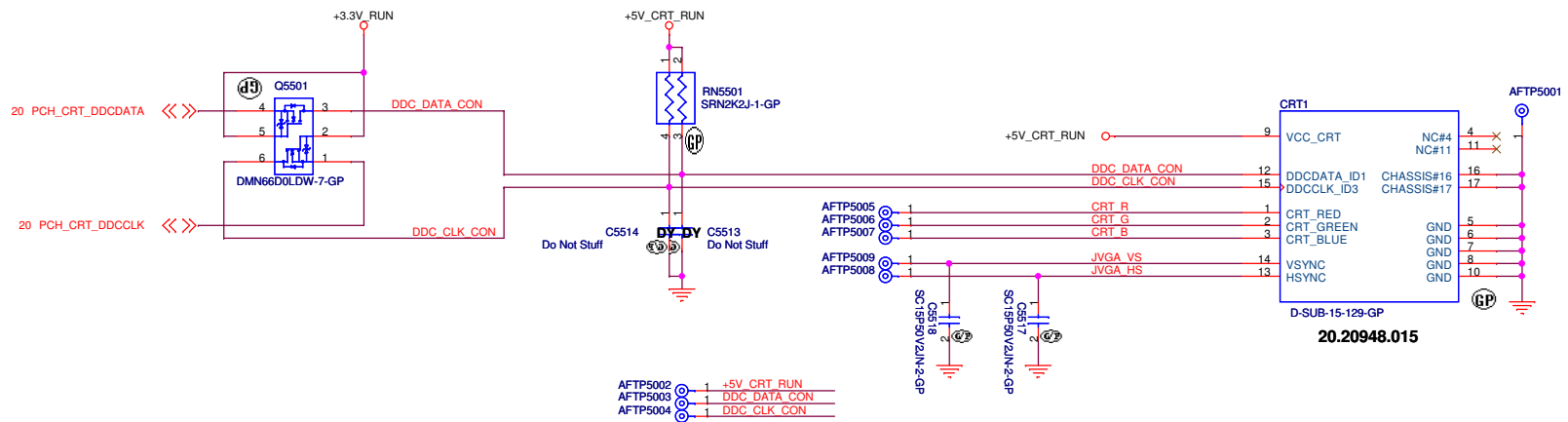
**Enrico/Caruso 15 CP**

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Date: Wednesday, April 13, 2011

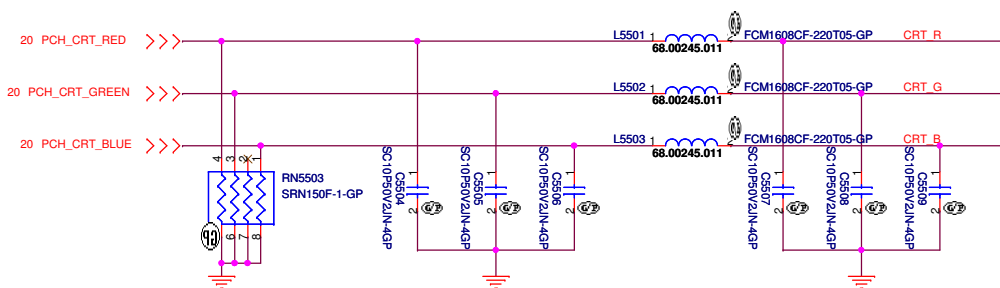
Sheet 54 of 99	Acc
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# SSID = VIDEO

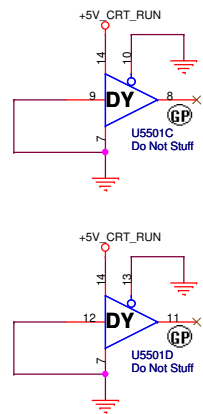
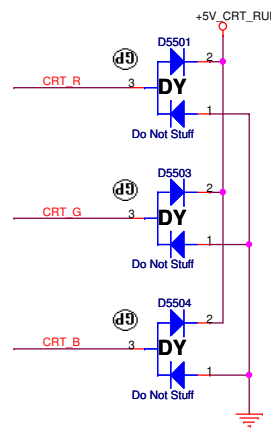
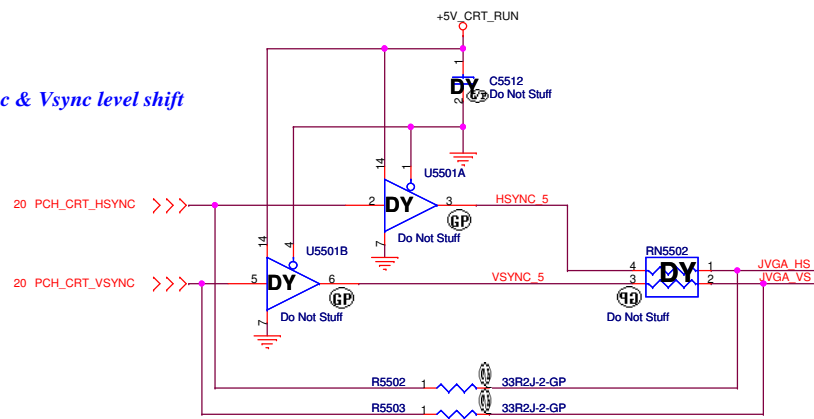


## Layout Note:

- \*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- \* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



## Hsync & Vsync level shift




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Title					
<b>CRT Connector</b>					
Size	Document Number				Rev
	<b>Enrico/Caruso 15 CP</b>				<b>A00</b>
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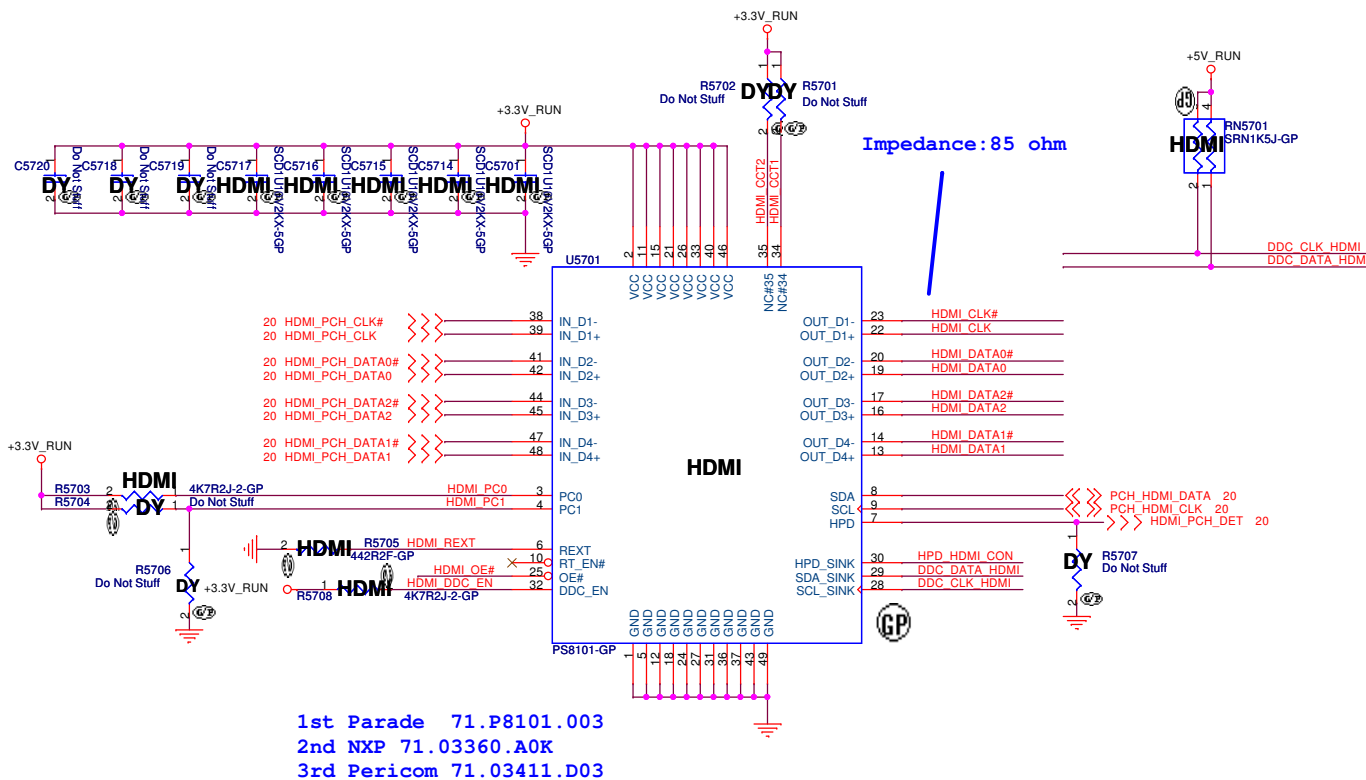
Sheet 56 of 99

Reserved



SSID = VIDEO

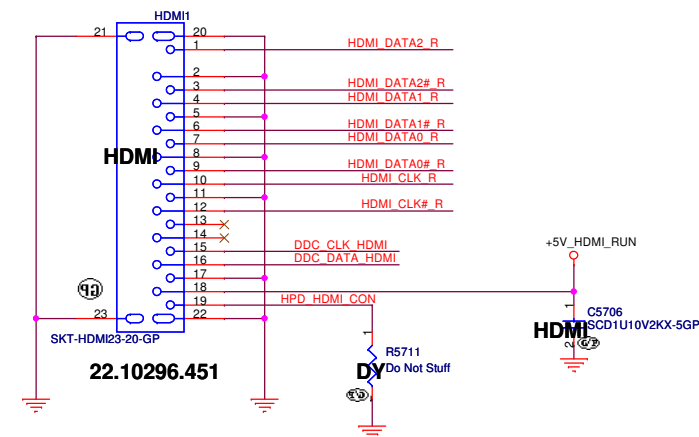
# HDMI Level Shifter & CONNECTOR



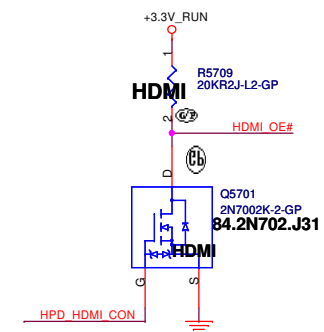
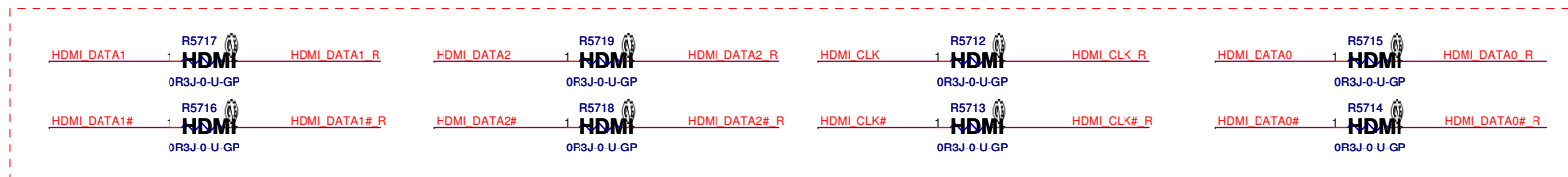
HDMI level shifter BOM controll table

		PS8101	PTN3360B	PI3VDP411LSR
PIN3	R5703	Stuff 4.7K_5%	DY	DY
PIN4	R5704	DY	DY	DY
PIN6	R5705	Stuff 499_1%	Stuff 10K_1%	DY
PIN10		NC	NC	NC

## HDMI CONN



A00-0412

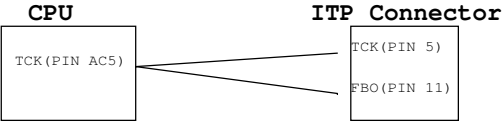


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SSID = User.Interface

ITP Connector

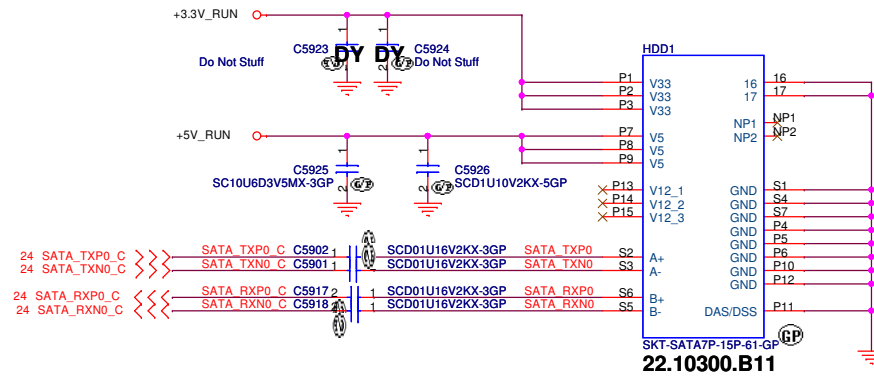
H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



REMOVE FAN CONNECTOR FOR HR THERMAL SOLUTION 7/12

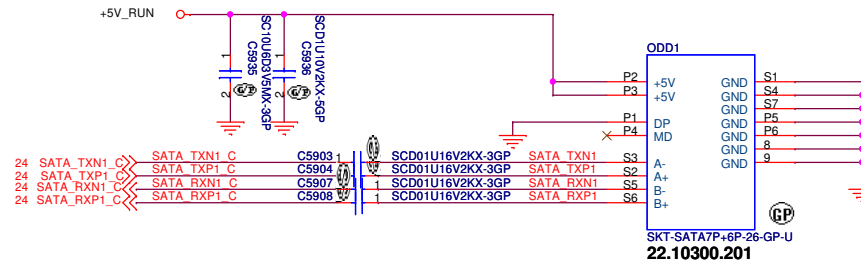
SSID = SATA

## SATA HDD Connector



## SATA ODD Connector

SATA\_RX- and SATA\_RX+ Trace  
Length match within 20 mil



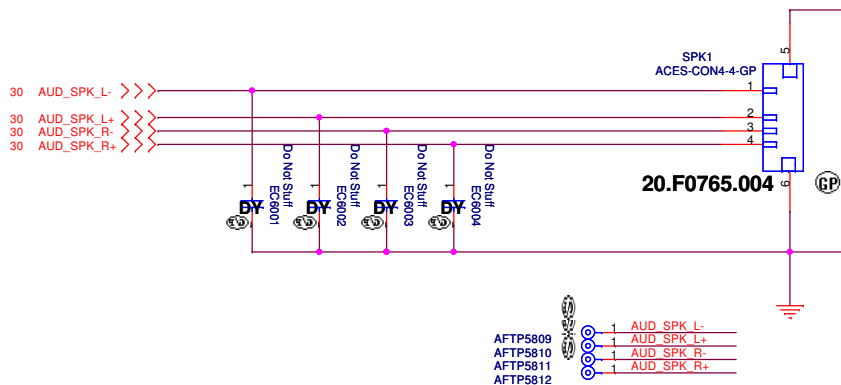
DV15 CP UMA second



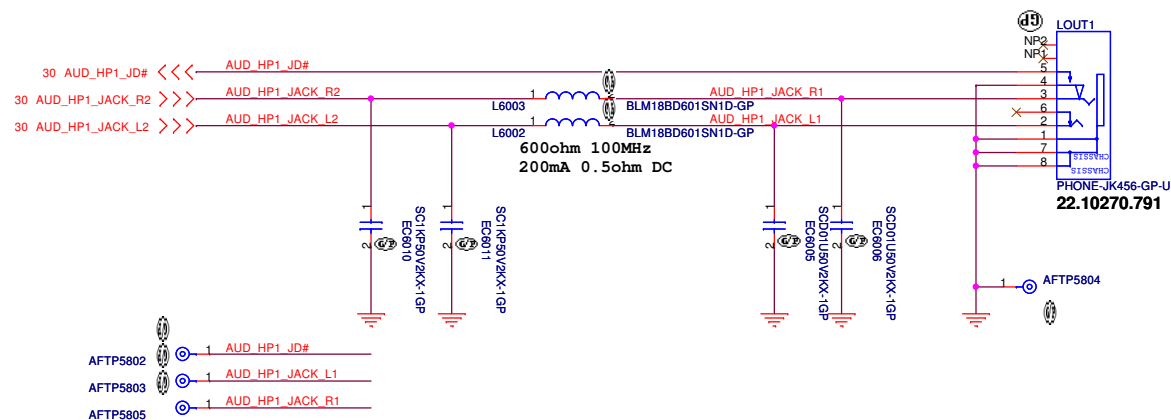
Title			
HDD/ODD			
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SSID = AUDIO

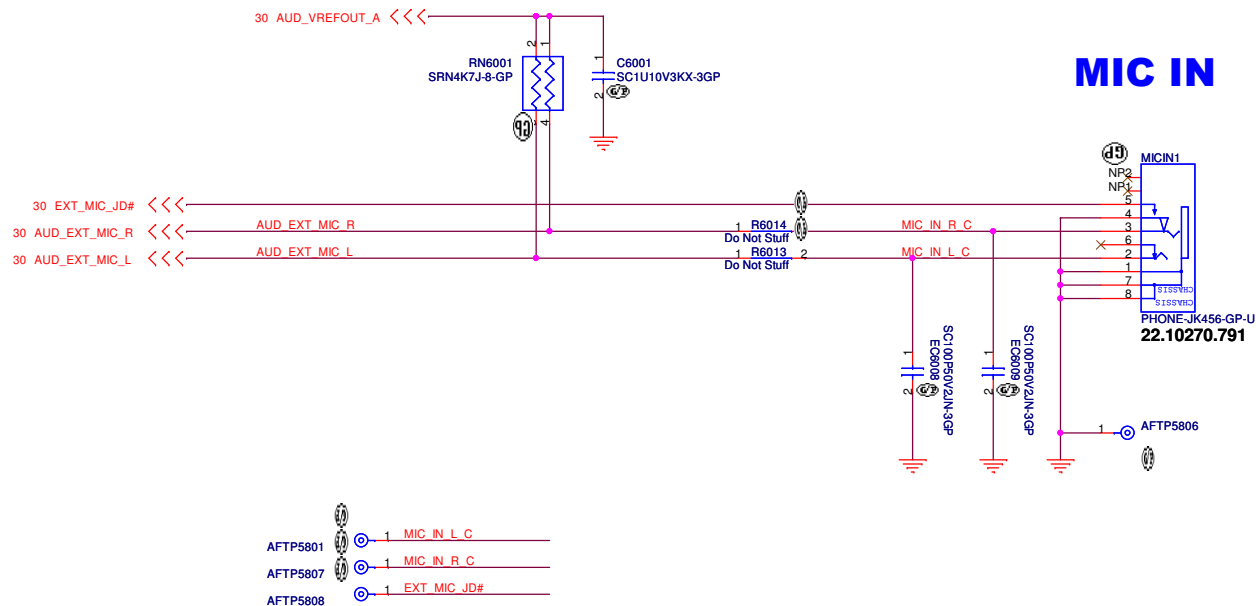
## Speaker Connector



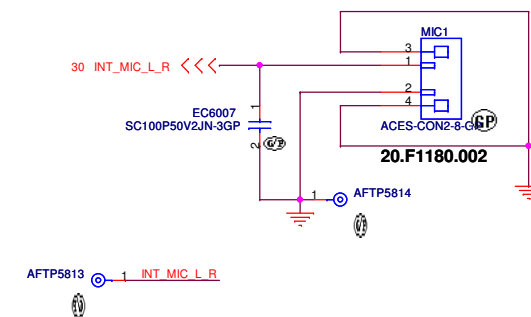
## LINE1 OUT



## MIC IN



## Internal Microphone

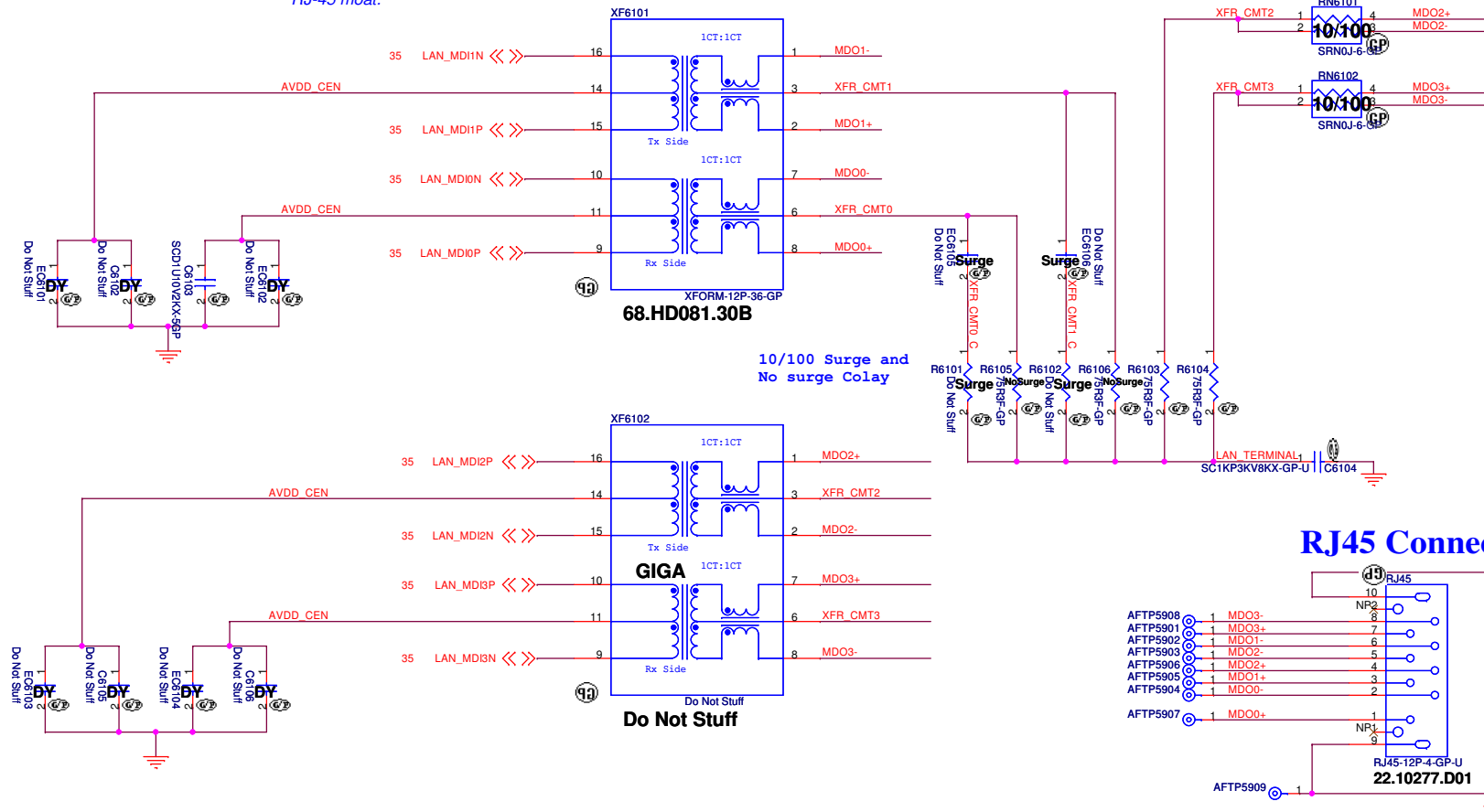


DV15 CP UMA second

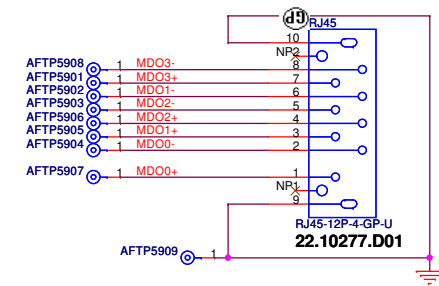
2009-10-1 Change MDI1+ (XF601.16) to MDI1+ (XF601.15)  
 Change MDI1- (XF601.15) to MDI1- (XF601.16)  
 Change MDI0+ (XF601.10) to MDI0+ (XF601.9)  
 Change MDI0- (XF601.9) to MDI0- (XF601.10)  
 Change RJ45-3 (XF601.1) to RJ45-3 (XF601.2)  
 Change RJ45-6 (XF601.2) to RJ45-6 (XF601.1)  
 Change RJ45-1 (XF601.7) to RJ45-1 (XF601.8)  
 Change RJ45-2 (XF601.8) to RJ45-2 (XF601.7)

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

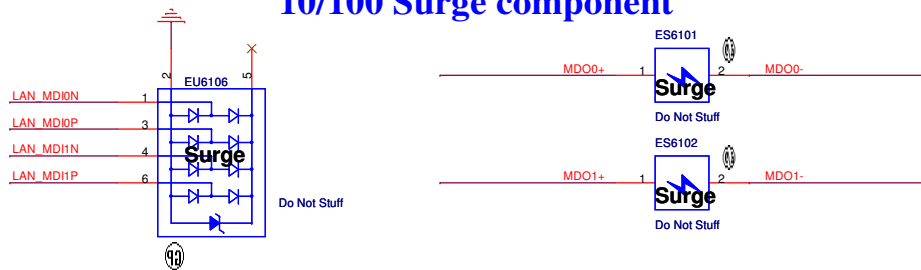
## 10/100M Lan Transformer



## RJ45 Connector



## 10/100 Surge component

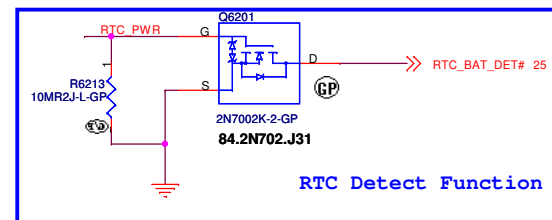
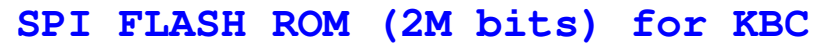


<Core Design>

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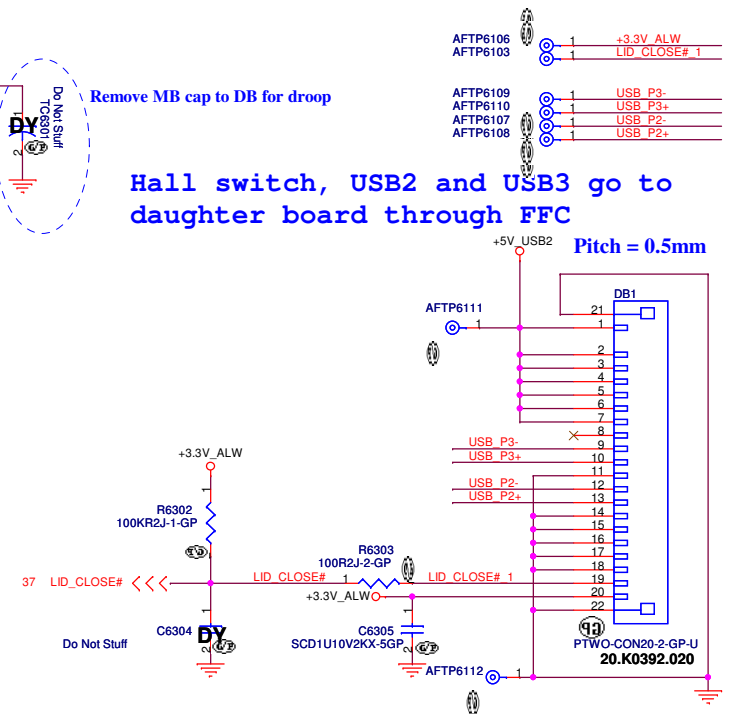
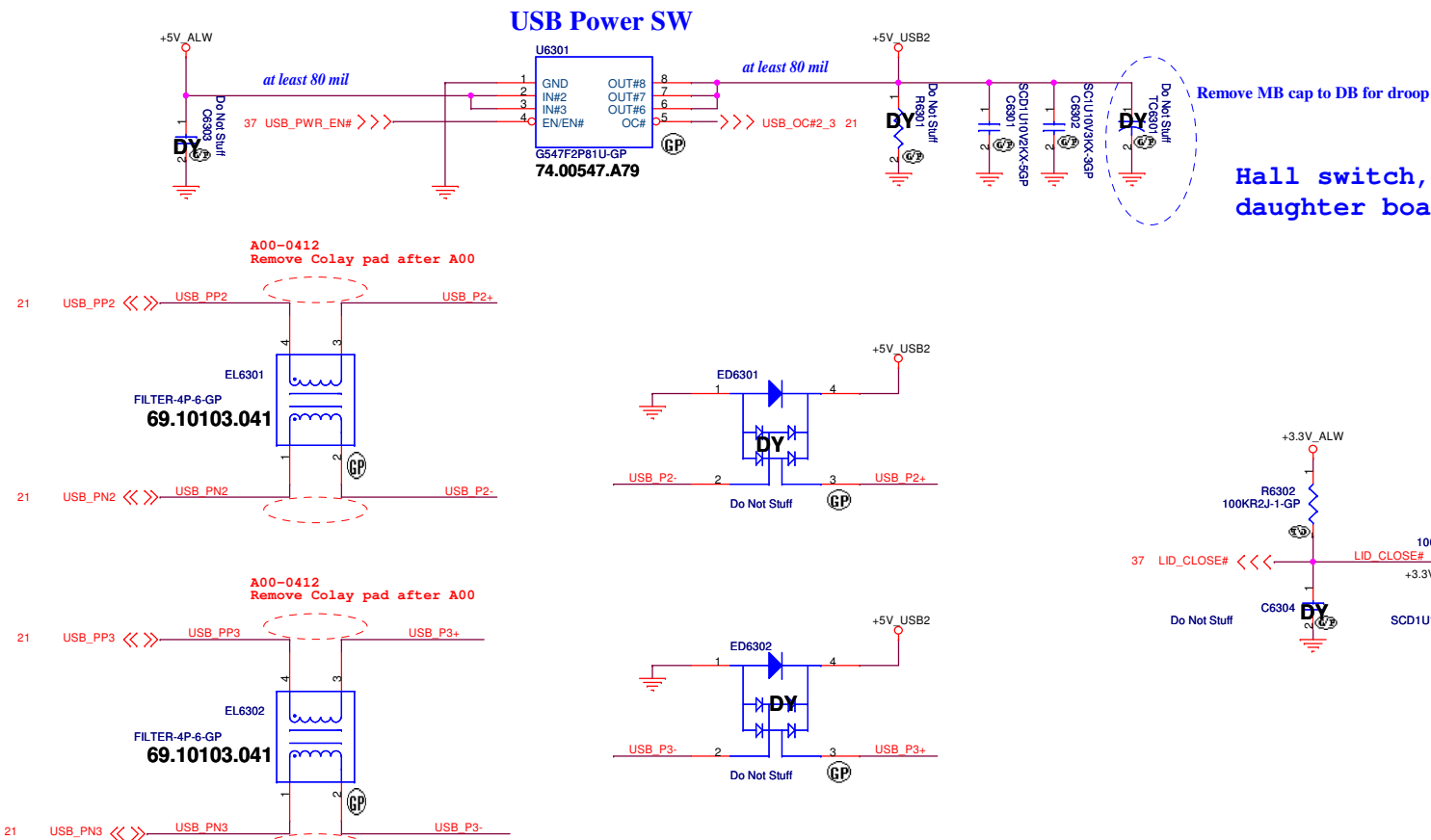
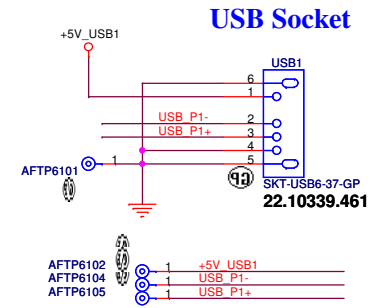
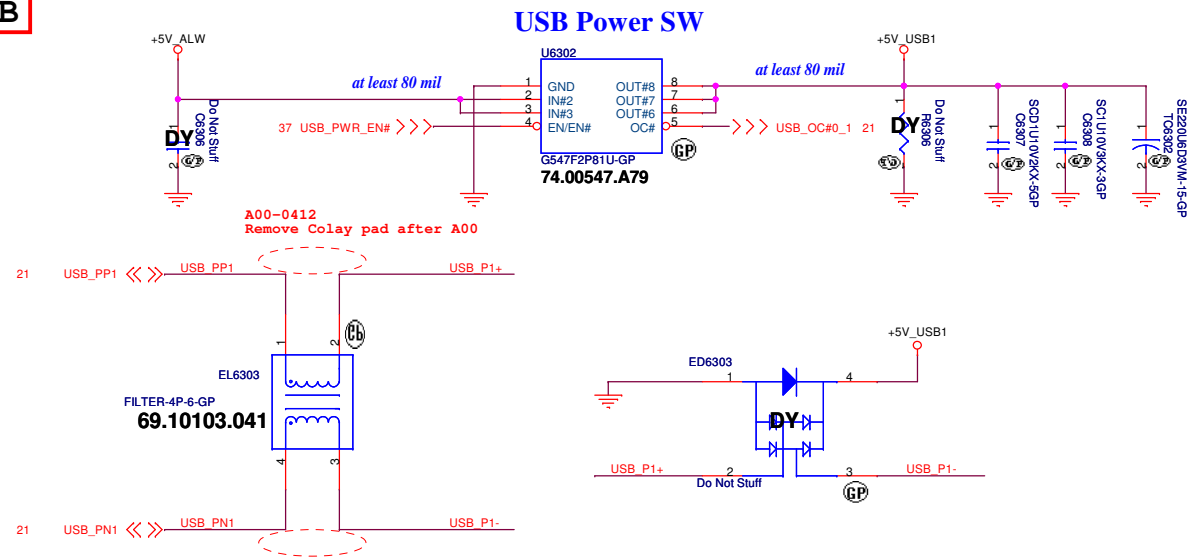
LAN Conn			
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**SPI FLASH ROM (32M bits) for PCH**



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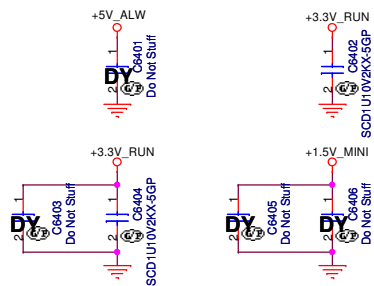
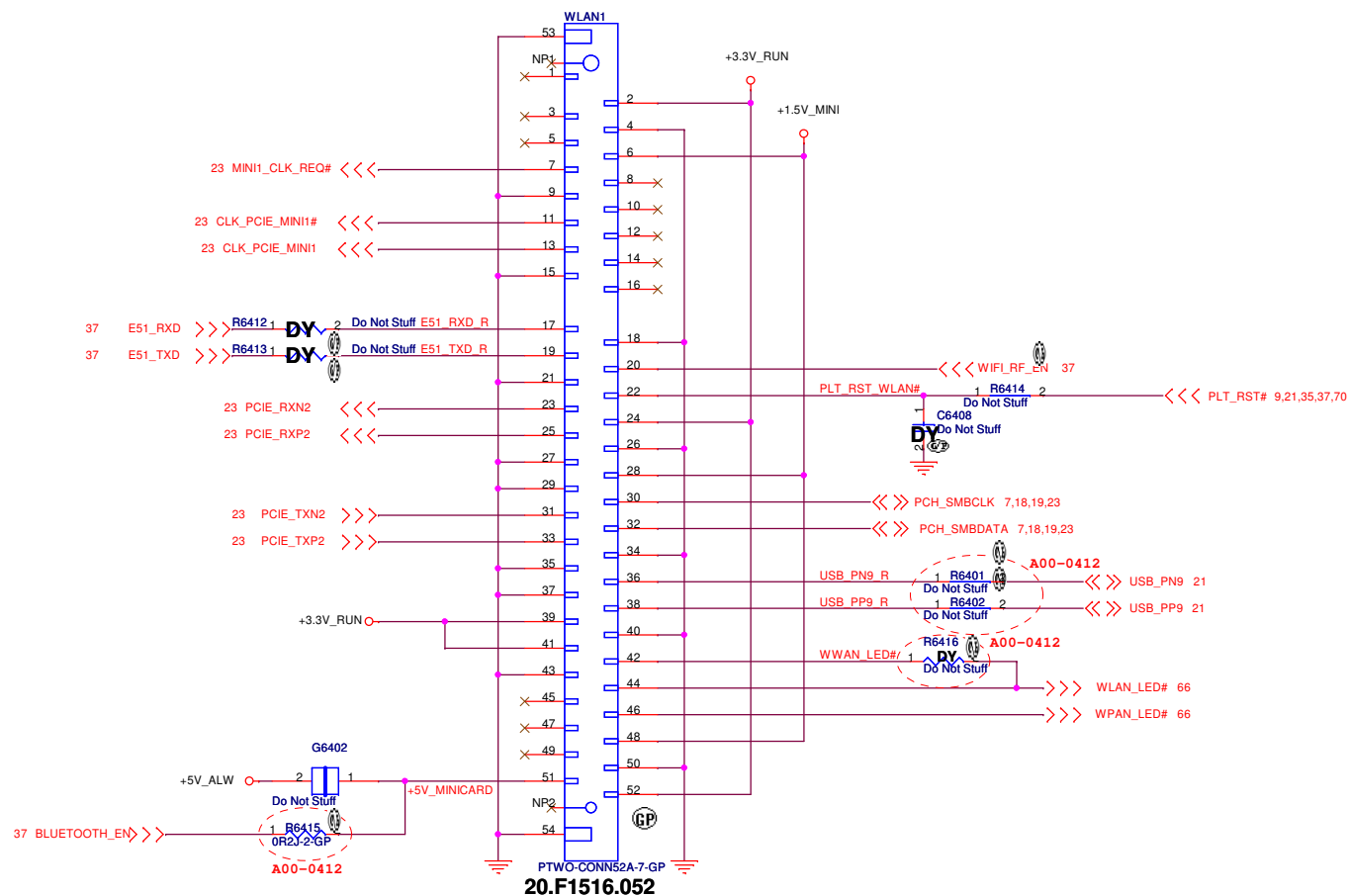
SSID = USB



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SSID = Wireless

## Mini Card Connector(802.11a/b/g)



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Title

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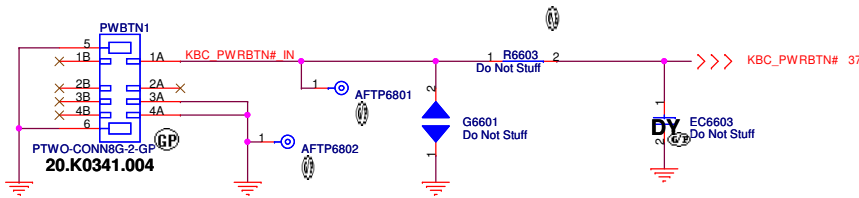
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SSID = User.Interface

## Power BTN Connector



LED Location from left to right  
(MB, Top View)

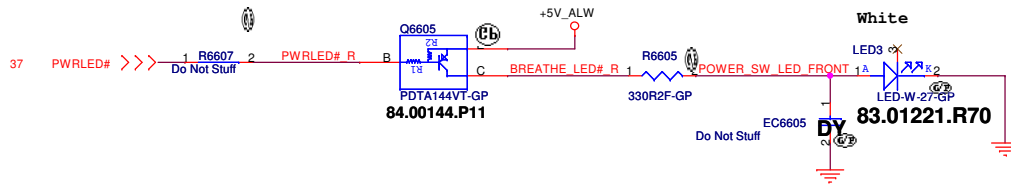
LED3  
PWR

LED2  
HDD

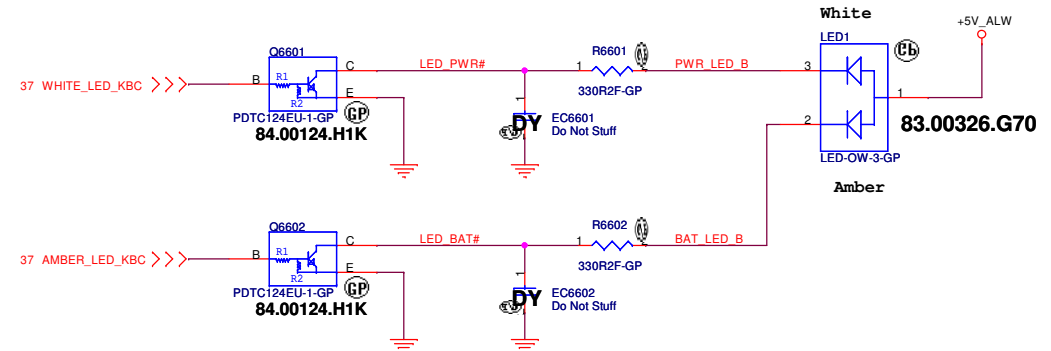
LED1  
Battery

LED4  
WLAN

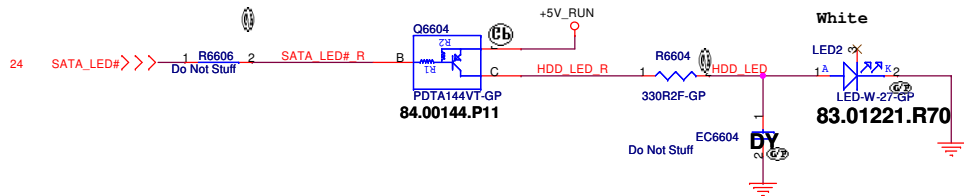
## POWER LED



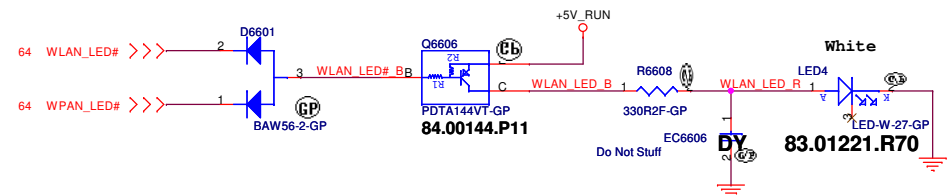
## Battery LED



## HDD LED




## WLAN LED



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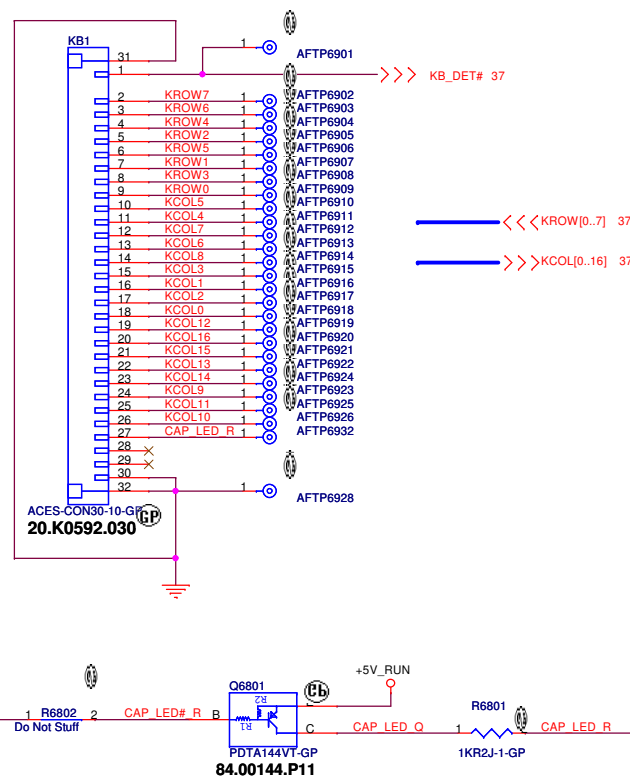
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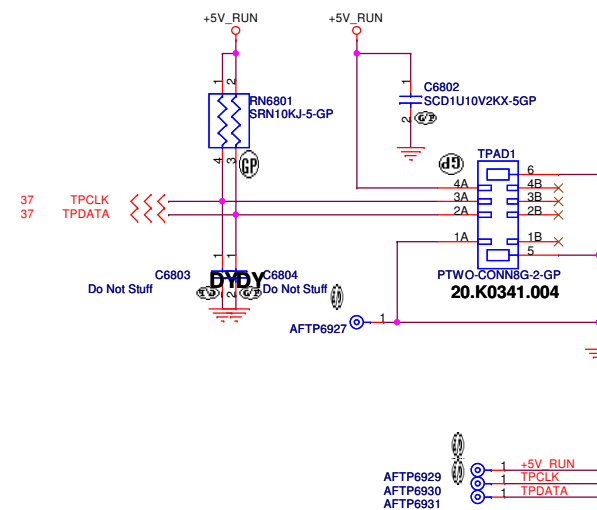
**SSID = KBC**

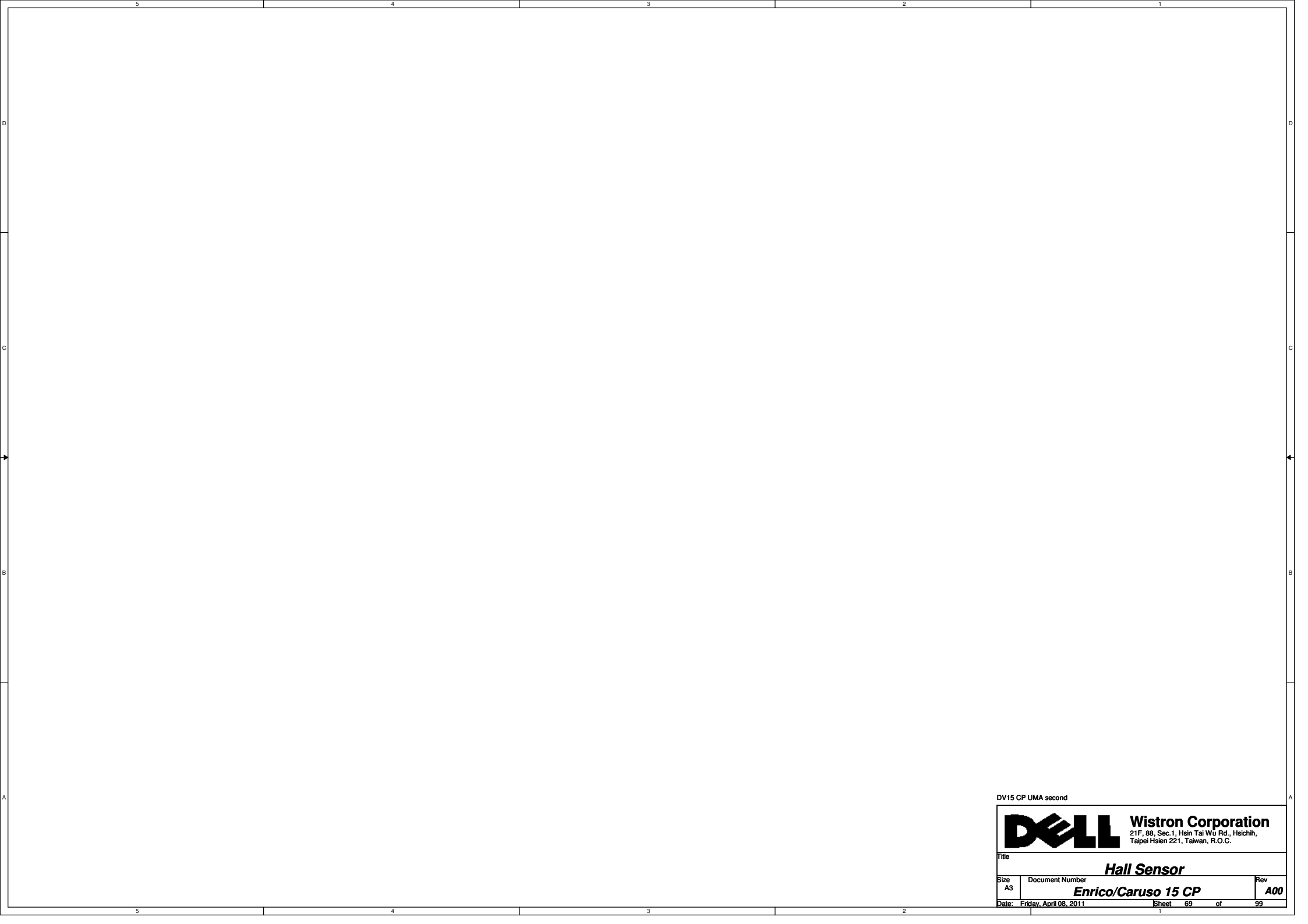
## Internal KeyBoard Connector




```
SSID = Touch.Pad
```

## TouchPad Connector





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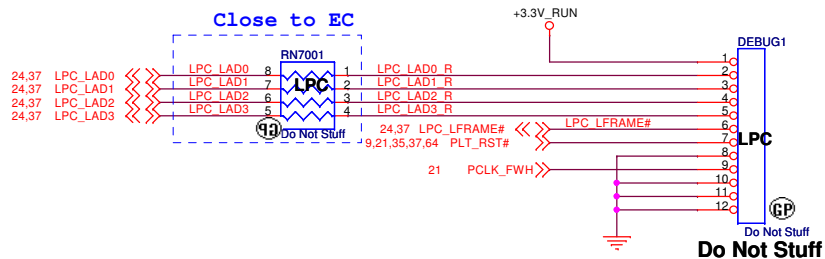
Wistron Corporation

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Title

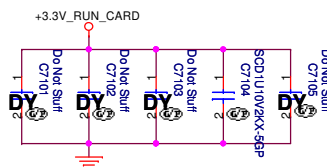
Hall Sensor

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## *SD/XD/MS Card Reader*



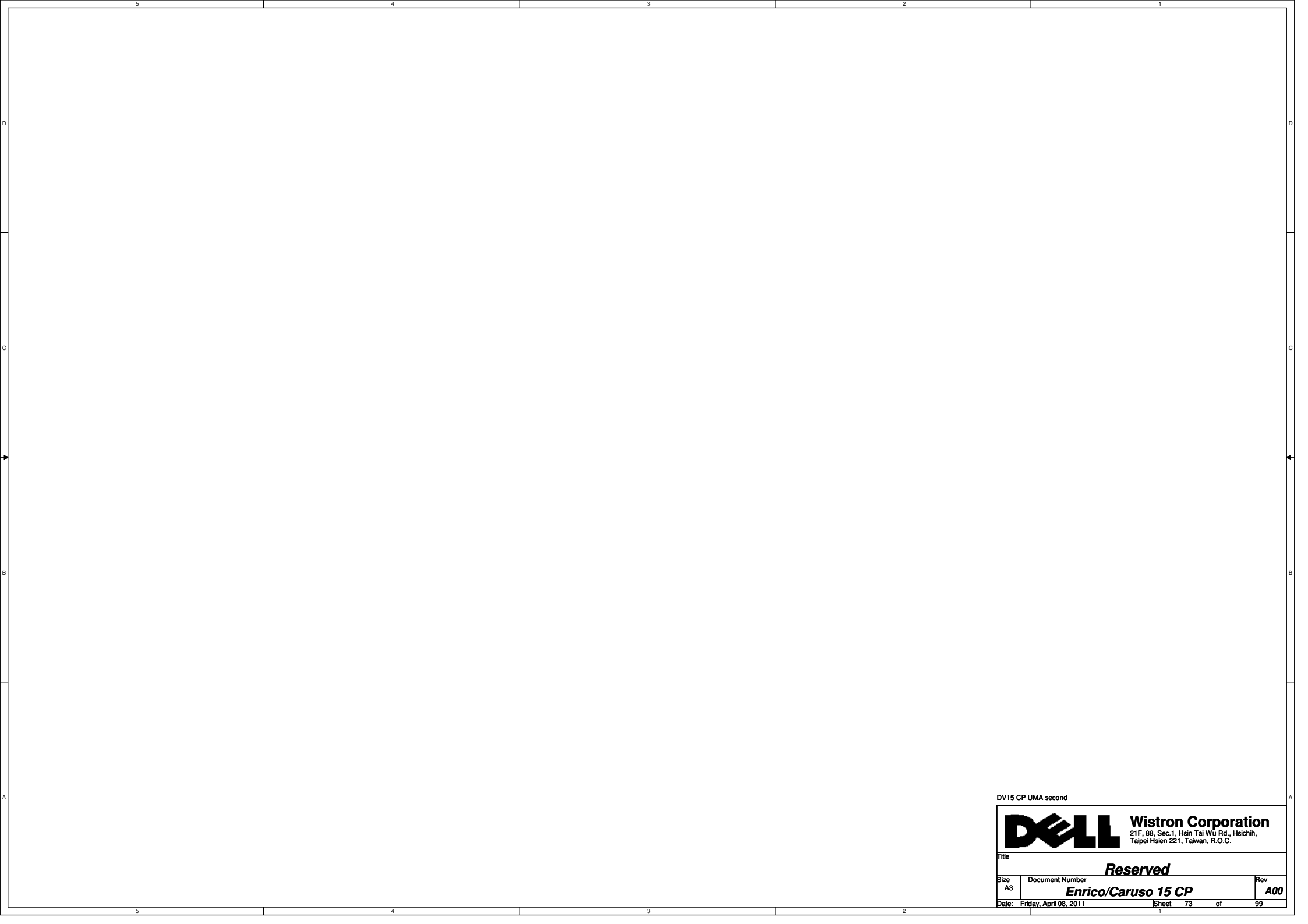
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<b><i>CARD Reader Connector</i></b>			
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Title

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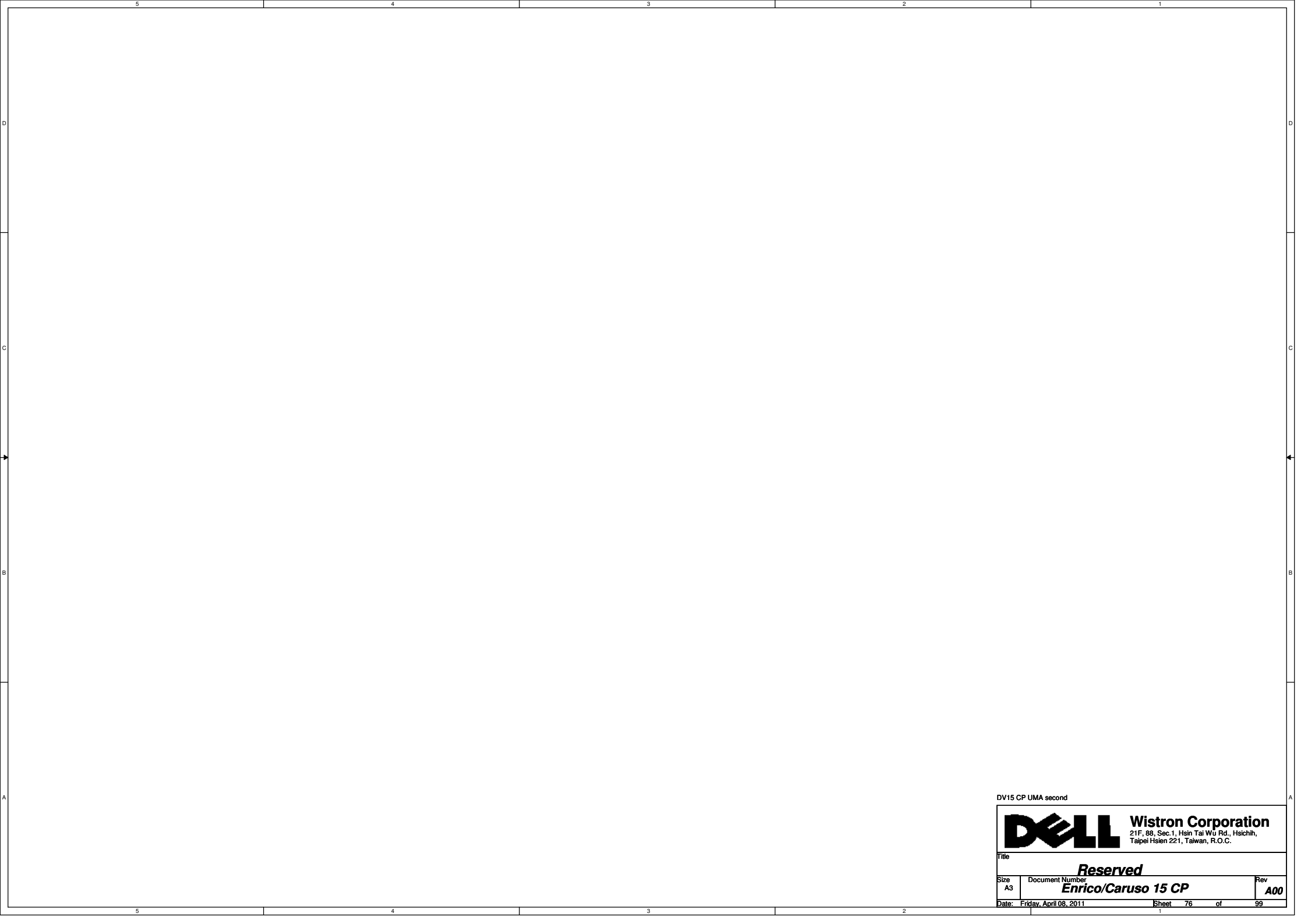
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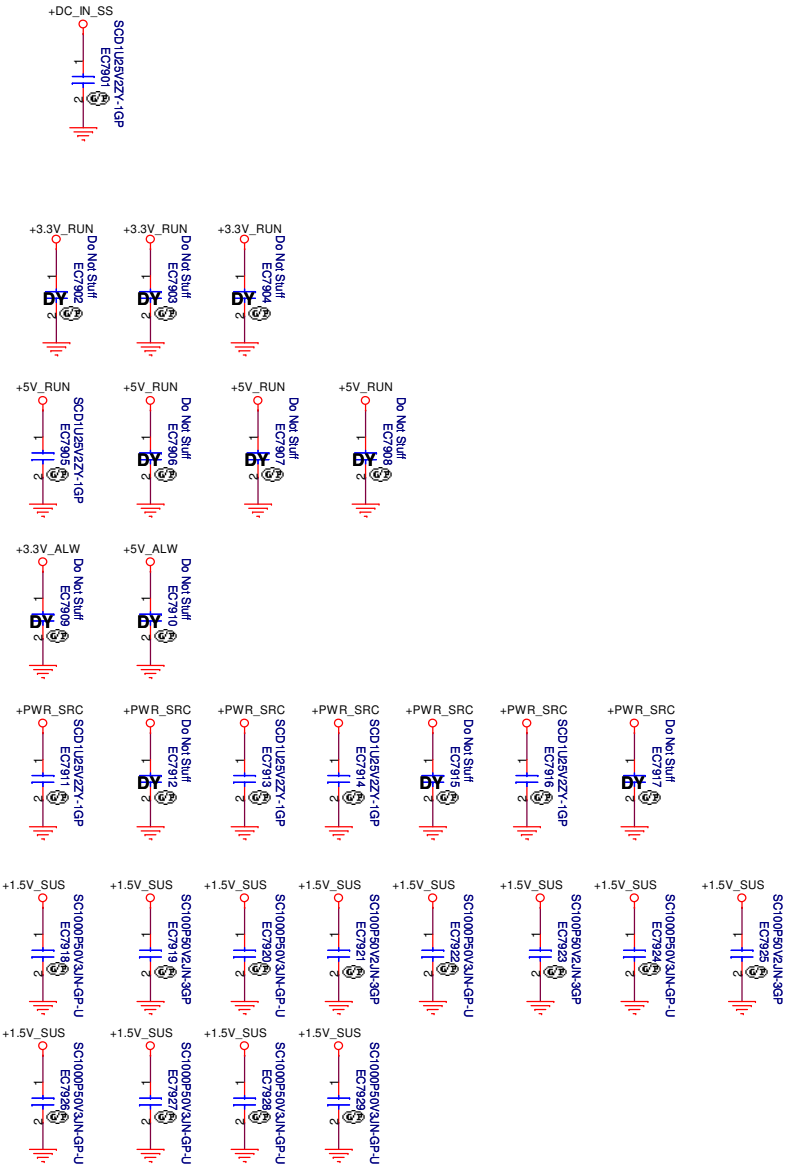
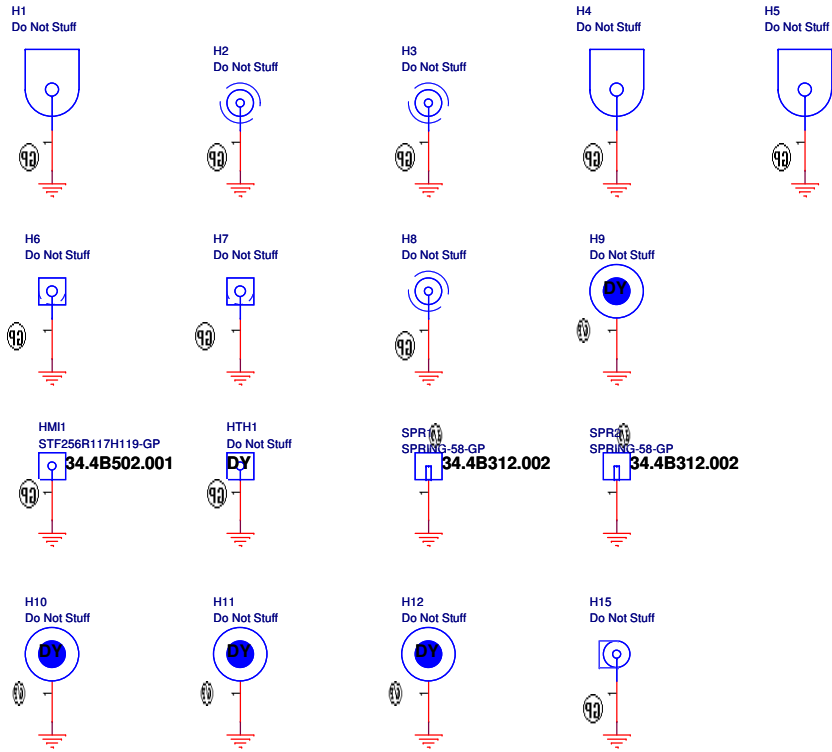
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SSID = Mechanical



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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Date	Time	Location	Activity	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks	Remarks

### UNUSED PARTS/EMI Capacitors

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Free
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SSID = VIDEO

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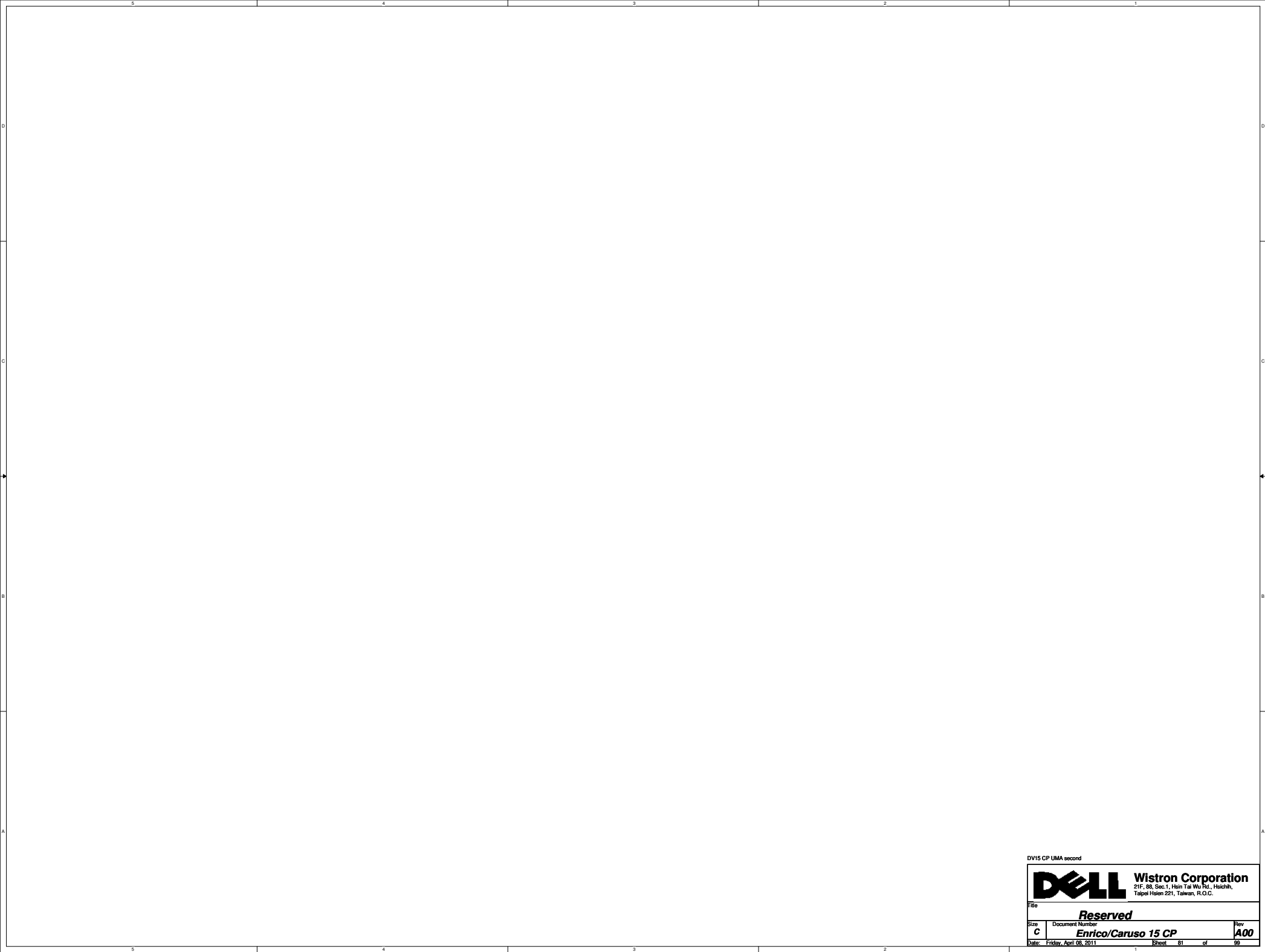
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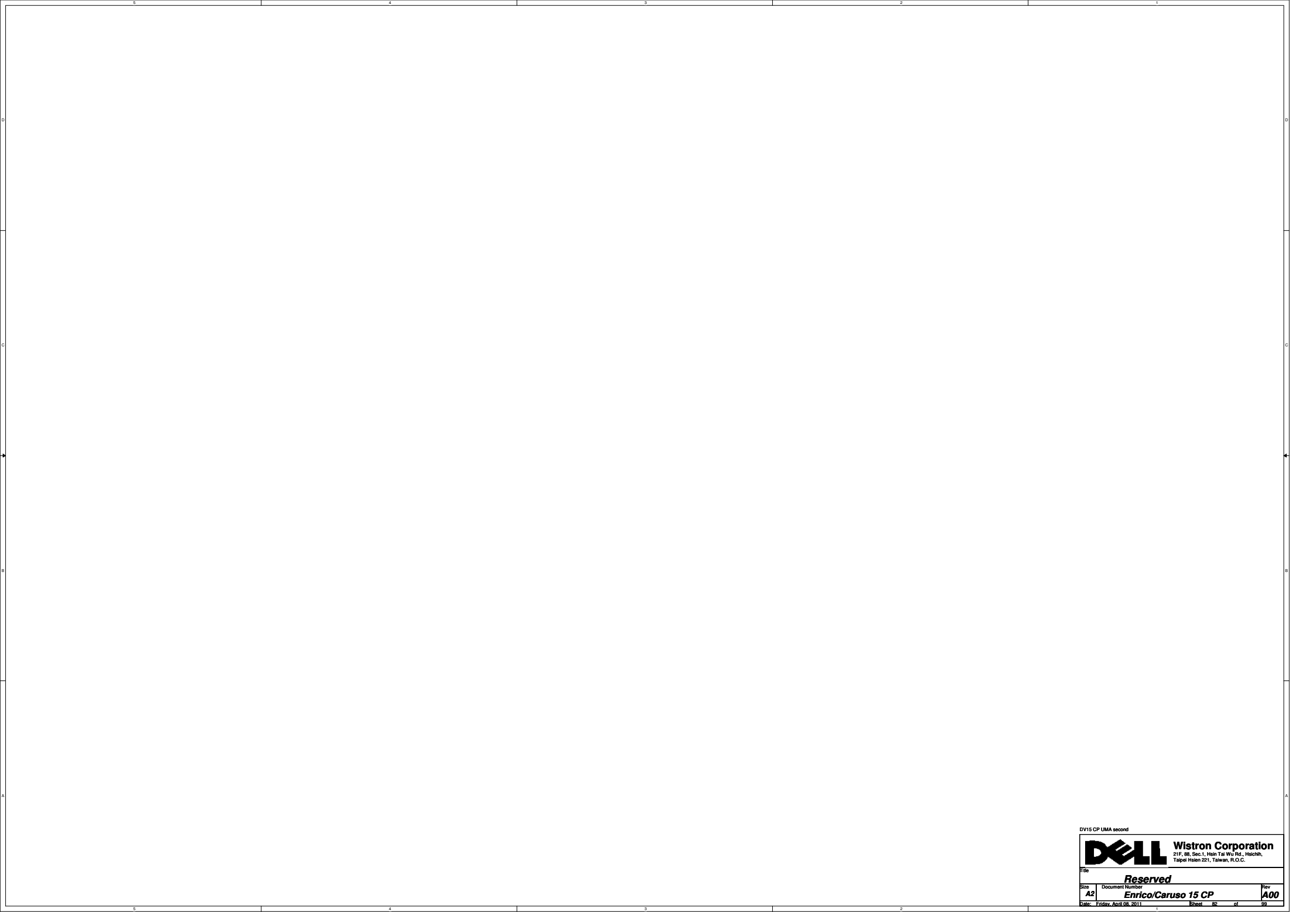
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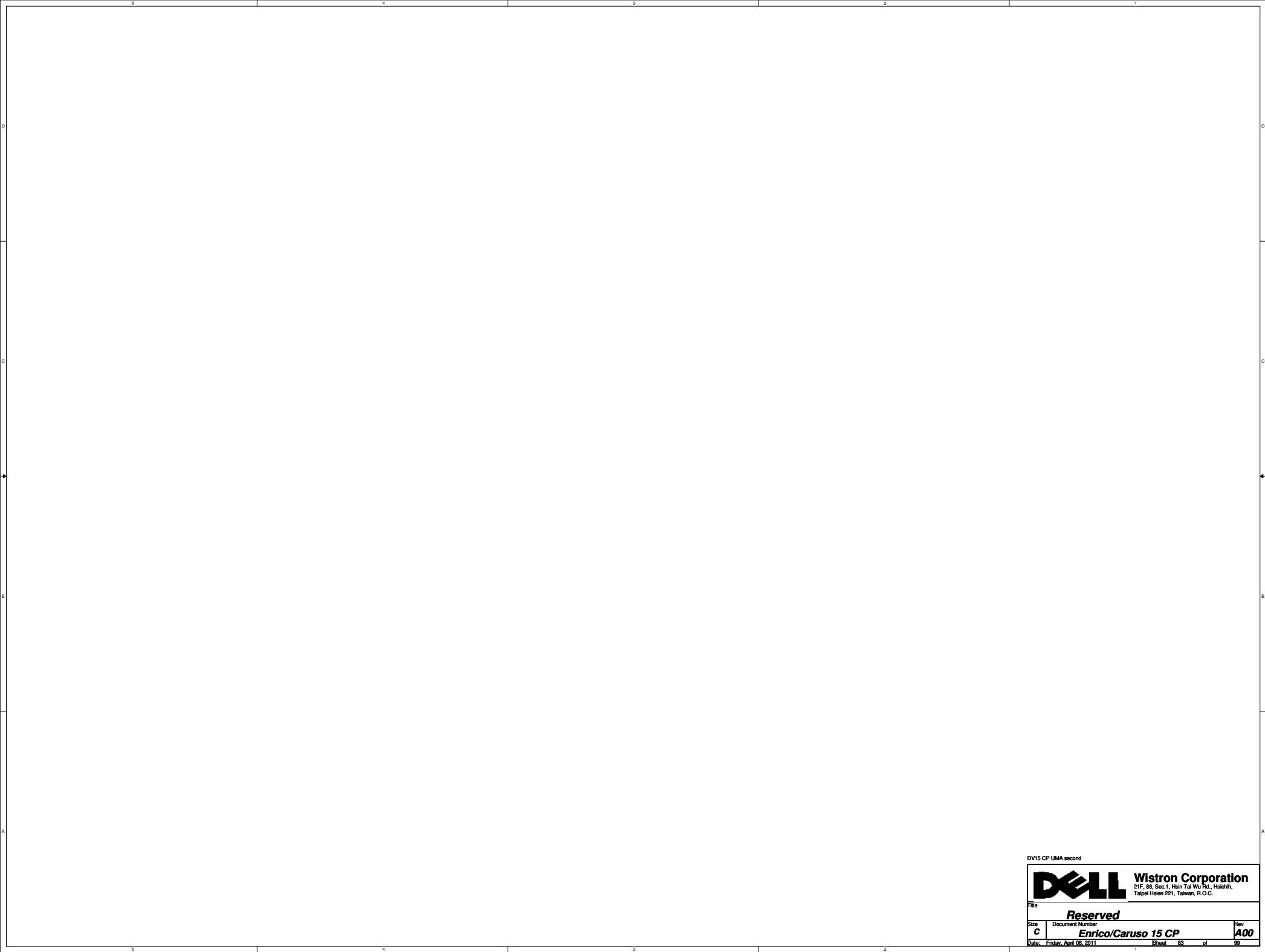


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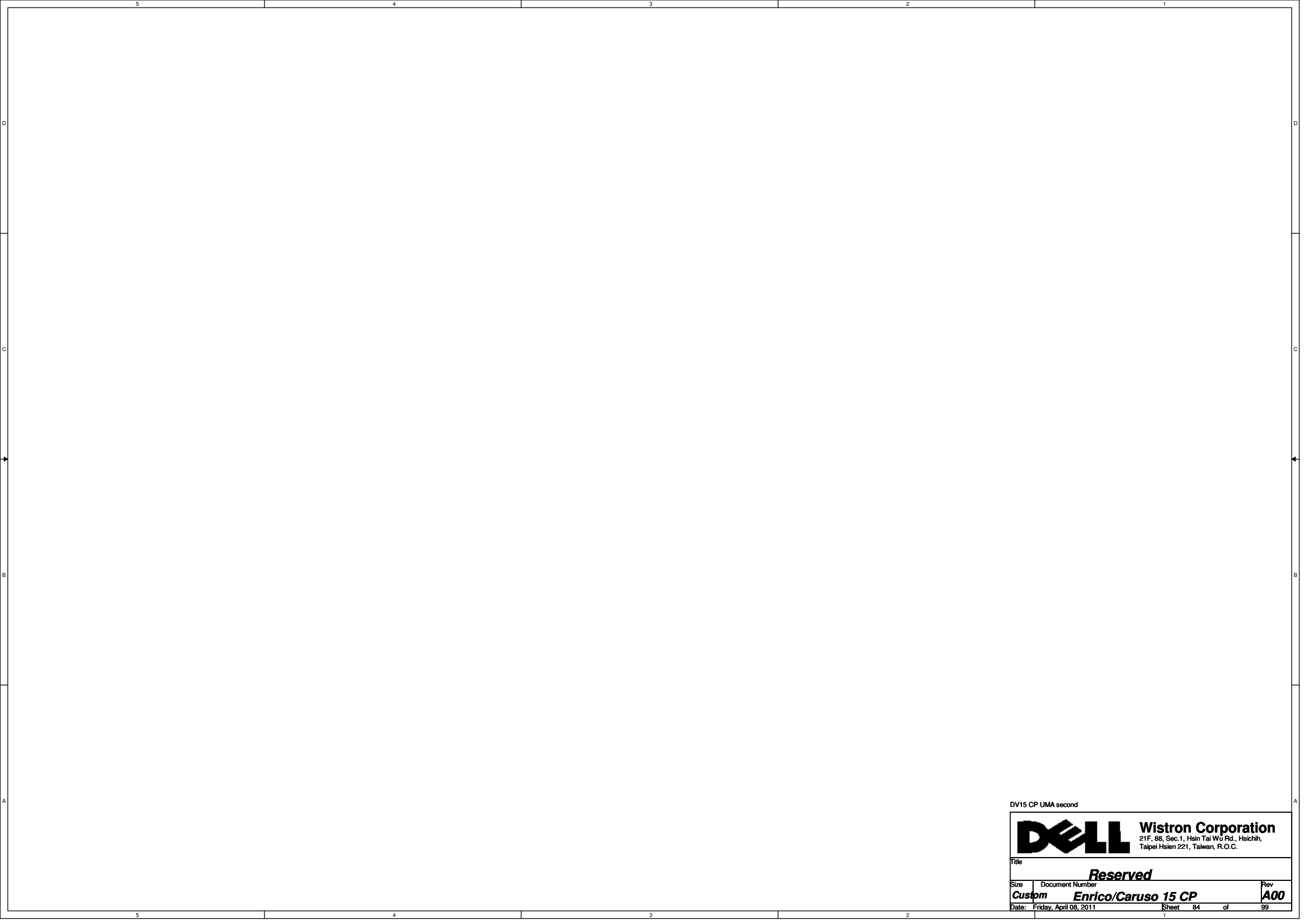


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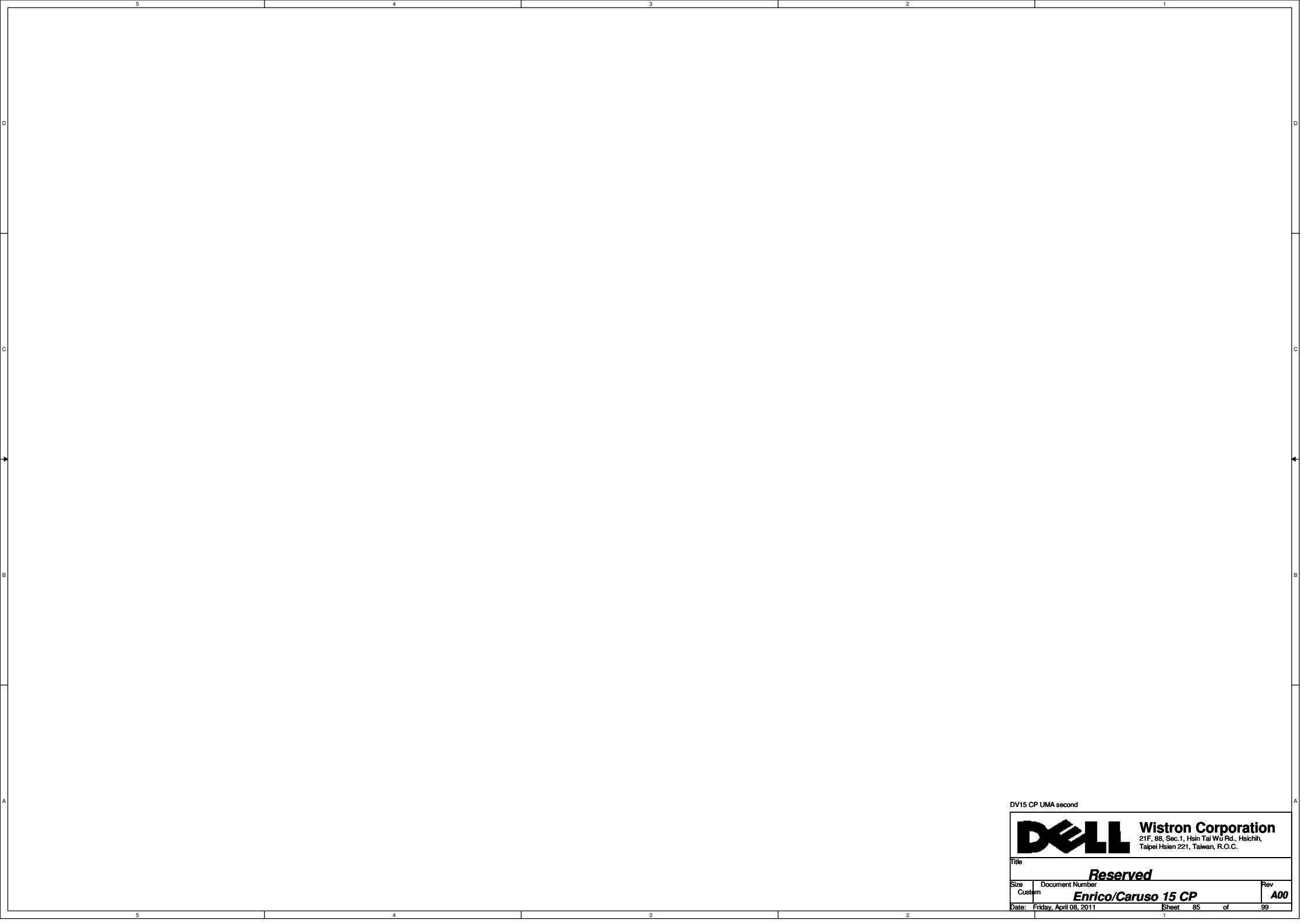
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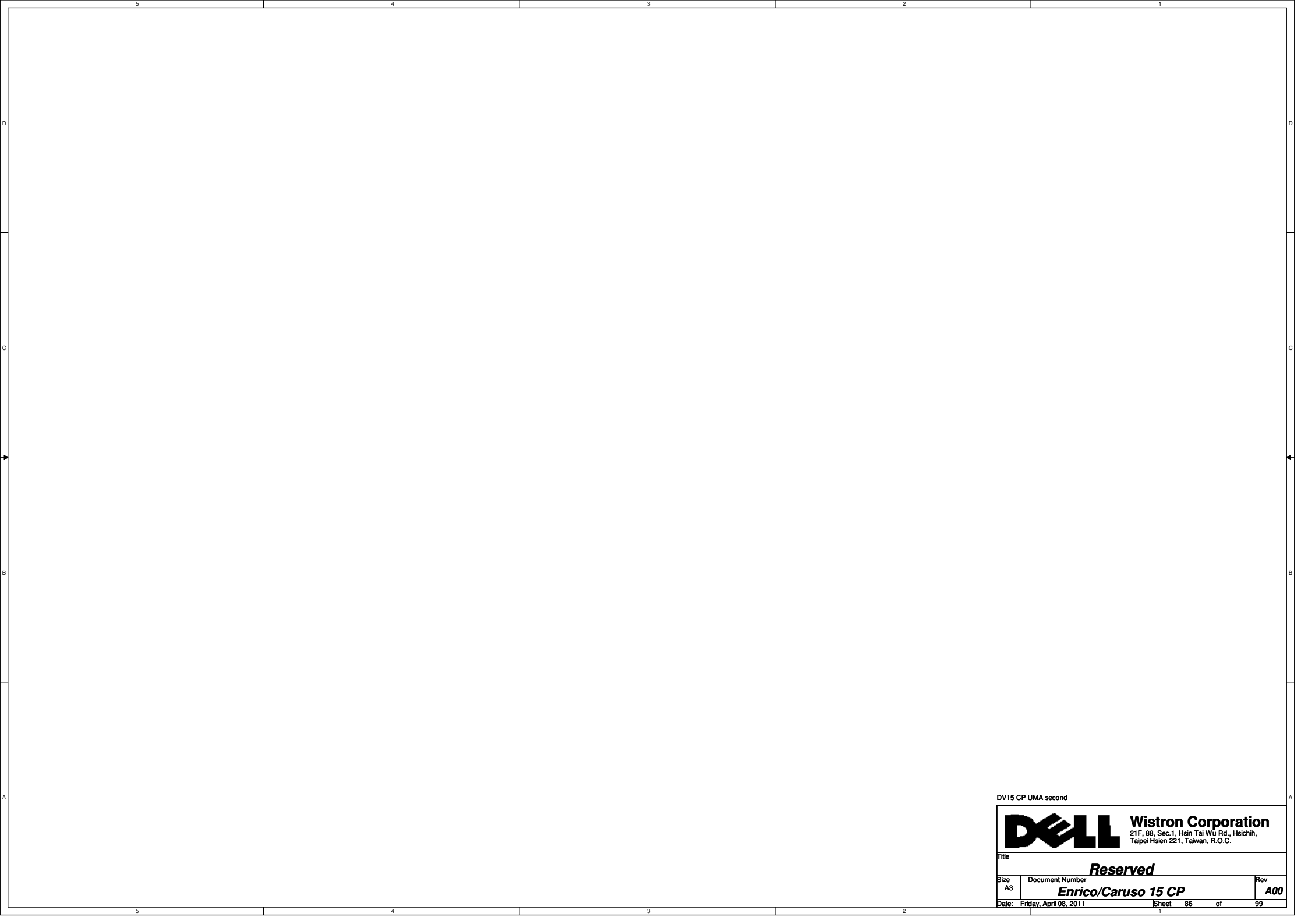
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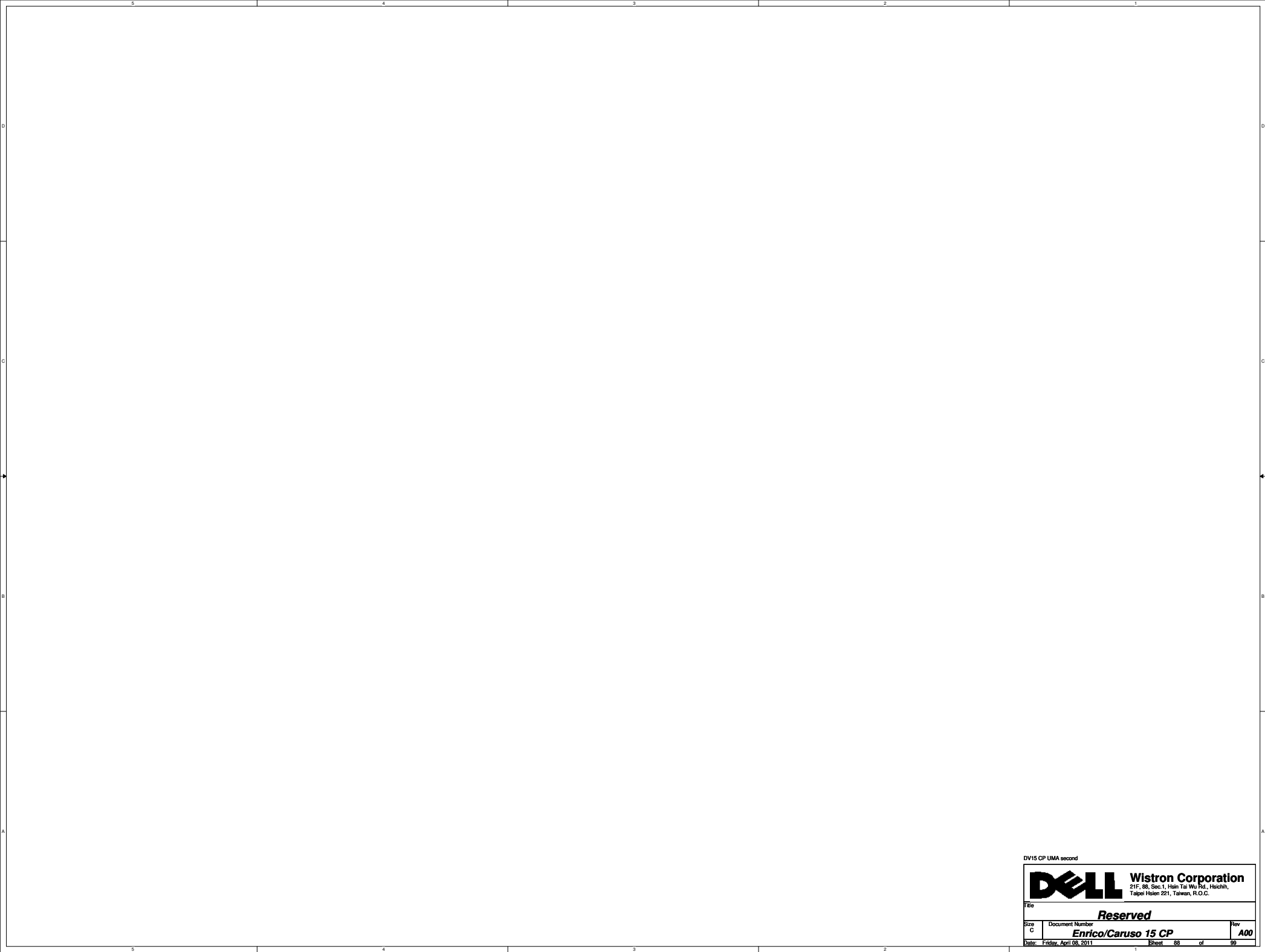


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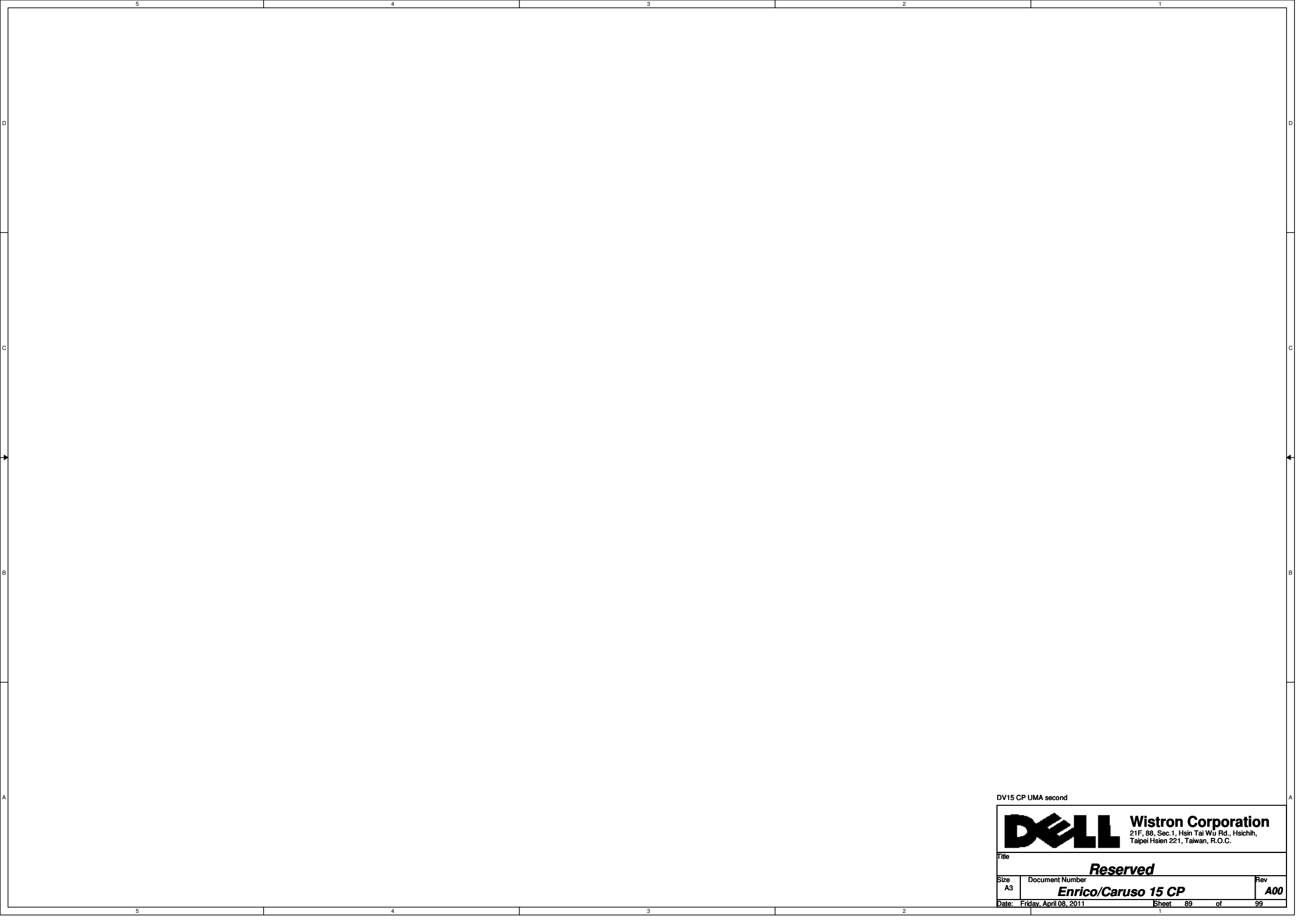
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(AC mode)

The diagram shows the timing relationships for KBC GPIO36 control and other signals. Key events include:

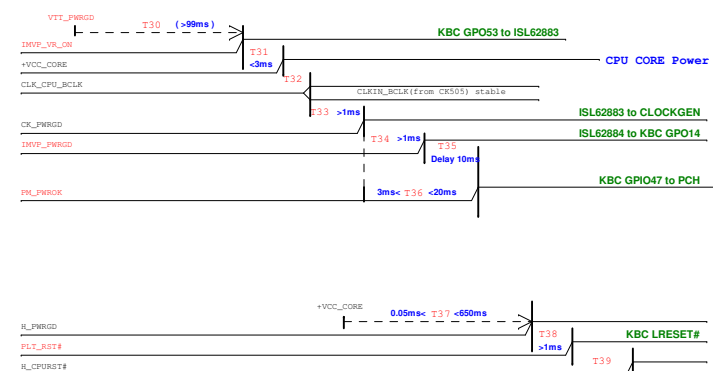
- RTN\_VCC** and **PCB\_RSTCRST#** signals.
- FWMS\_SSC** signal.
- +3.3V\_RTC\_LDO** signal.
- SS\_DISABLE** signal.
- +5V\_ALW** and **+3.3V\_ALW** signals.
- +15V\_ALW** signal.
- SV\_POR** signal.
- SUS\_PWR\_ON\_ACK** signal.
- PCB\_RSBSST#** (EC delay 40ms) signal.
- PCB\_RSBSCLK\_KBC** signal.
- AC\_PRESENT\_EC** signal.
- Press Power button** event.
- KBC\_PWRBTN\_EC#** and **KBC\_PWRBTN\_EC# GPIO3** signals.
- AC\_PML\_PWRBTN#** and **KBC GPIO84 to PCH** signals.
- AC\_PML\_PWRBTN#** signal.
- PM\_SLP\_S4#** and **PM\_SLP\_S3#** signals.
- PM\_LAN\_DISABLE** signal.
- +3.3V\_LAN** and **+1.5V\_SUS** signals.
- +V\_DDR\_REF (0.9V)** signal.
- +5V\_RUN** and **+3.3V\_RUN** signals.
- +1.5V\_RUN** signal.
- RUNPWROK** signal.
- +1.5V\_VTT** signal.
- VTT\_PWROK** (after delay 1ms GP196-VDDPWROOD\_EC output for s3 reduction) signal.
- +0.75V\_SDR\_VTT** signal.
- GFX\_VR\_EN** signal.
- +CPU\_GFX\_CORE** signal.
- IL\_VTTPWROK** signal.

Timing points T1 through T29 are marked on the signals. Annotations include:

- KBC GPIO36 control**
- TPS51125 to KBC GPIO46**
- PCH to KBC GPIO94**
- KBC GPIO43 to PCH**
- PCH to KBC GPIO00**
- KBC GPIO16 to LAN**
- TPS51218 to KBC GPI34**

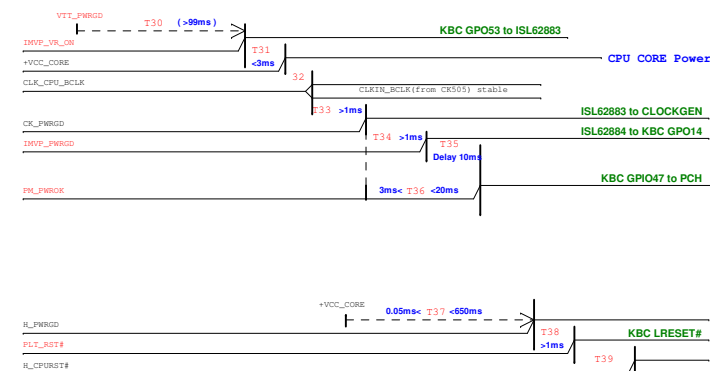
Timing constraints are specified:

- T11 < 200ms**
- T14 > 30us**
- T18 > 10ms**
- +5V\_RUN and +3.3V\_RUN need meet 0.7v difference**



(DC mode)

Timing diagram for the PCH to KBC GPIO16 transition. The diagram shows the sequence of signals from the PCH to the KBC, including the press of the power button. Key signals include RTC\_VCC, PCH\_RICRST#, PWR\_SRC, +3.3V\_RTC\_LDO, KBC\_PWRBTN\_EC#, KBC\_PWRBTN\_EC# GPIO3, EC\_ENABLE# (GPIO51) keep low, KBC\_GPIO36 control, +KBC\_PWR, S5\_ENABLE, +5V\_ALW, +3.3V\_ALW, +15V\_ALW, 3V3\_V5V\_POK, PCH\_PWRBTN#, S5H\_PWRBTN\_ACK, PCH\_RIMRST#, PCH\_SUSCLK\_KBC, DC PCH\_RIMRST#, PCH\_SLP\_S4#, PCH\_SLP\_S3#, PCH\_LAN\_ENABLE, +3.3V\_LAN, +1.5V\_S0S, +V\_DDR\_REF (0.9V), +5V\_RUN, +3.3V\_RUN, +1.5V\_RUN, +1.8V\_RUN, RUNPWROK, +1.05V\_VTT, VTT\_PWDG0 (after delay 1ms GPT96+VDDPWROD0\_EC output for s3 reduction), +0.75V\_DDR\_VTT, GFX\_VR\_EN, +CPU\_GFX\_CORE, and N\_VTTPWROD. The diagram is divided into two sections: the first section shows the initial power-up sequence from the PCH to the KBC, and the second section shows the transition from S4 to S3 state. Key timing points are marked with T1 through T29. Annotations include 'Press Power button', '+5V\_ALW + +3.3V\_ALW need meet 0.7V difference', 'TPS51125 to KBC GPIO46', 'KBC GPIO84 to PCH', 'PCH to KBC GPI94', 'KBC GPIO43 to PCH', 'PCH to KBC GPIO01', 'KBC GPIO16 to LAN', and 'TPS51218 to KBC GPI34'.



Item	Pg.	Date	Description	Owner
KBC	37	A00-0412	stuff R3722 and DY R3725 for change MB version from X02 to A00	EE
WLAN	64	A00-0412	change R6415 from short pad to 0 ohm for debug	EE
USB	54, 63	A00-0412	Remove colay pad(R5403,R5404,R6315,R6316,R6317,R6318,R6319,R6320) after A00	EMI
USB	32, 64	A00-0412	Remove colay pad(EL3201,EL6401) and short pad(R3204,R3205,R6401,R6402) after A00	EMI
CLK GEN	7	A00-0412	change R710~R717 from 0 ohm to short pad	EMI
HDMI	57	A00-0412	Remove colay pad(EL5701,EL5702,EL5703,EL5704) after A00	EMI
short pad	ALL	A00-0412	change PR4519,PR5006,PR5111,R3202,R3742,R3743,R3744,R7105 from 0 ohm to short pad	EE
RTC	62	A00-0412	change U6203 P/N to 83.R0304.B81 for RTC detect leakage issue	EE
RT8237A_+1.05V	49	A00-0412	update PU4901 symbol for part manager footprint change	POWER
WLAN	64	A00-0412	add and DY R6416 0 ohm for Wimax future	EE
POWER GAP	ALL	A00-0413	change power GAP (PG4511,PG4602,PG4604,PG4605,PG4606,PG4615,PG4617,PG4619,PG4621,PG4624,PG4625,PG4607,PG4608,PG4609,PG4622,PG4626,PG4627,PG4610,PG4611,PG4612,PG4613,PG4614,PG4616,PG4618,PG4620,PG4902,PG4903,PG4904,PG4905,PG4906,PG4908,PG4910,PG4911,PG4913,PG4915,PG4917,PG4919,PG4925,PG4926,PG4920,PG4927,PG4928,PG4929,PG4909,PG4901,PG4912,PG4914,PG4916,PG4918,PG5001,PG5012,PG5002,PG5003,PG5004,PG5008,PG5009,PG5010,PG5011,PG5013,PG5015,PG5016,PG5017,PG5104,PG5106,PG5301,PG5303,PG5305,PG5308,PG5311) P/N from ZZ.CON2d.XXX to ZZ.CLOSE.001 for PSE requests	POWER
Thermal	39	A00-0422	stuff R3904 to change T8 temperature setting for reliability test	EE

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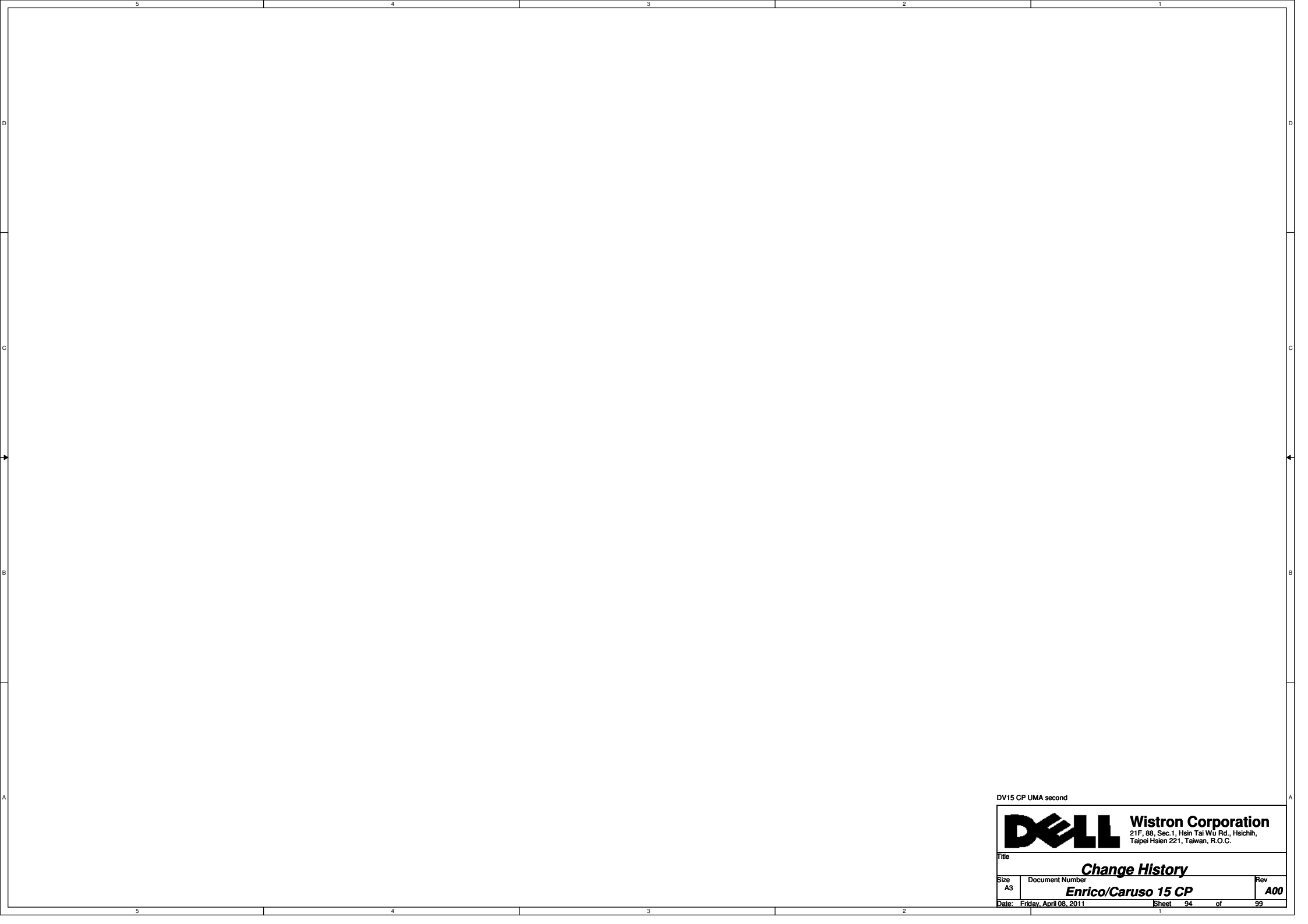
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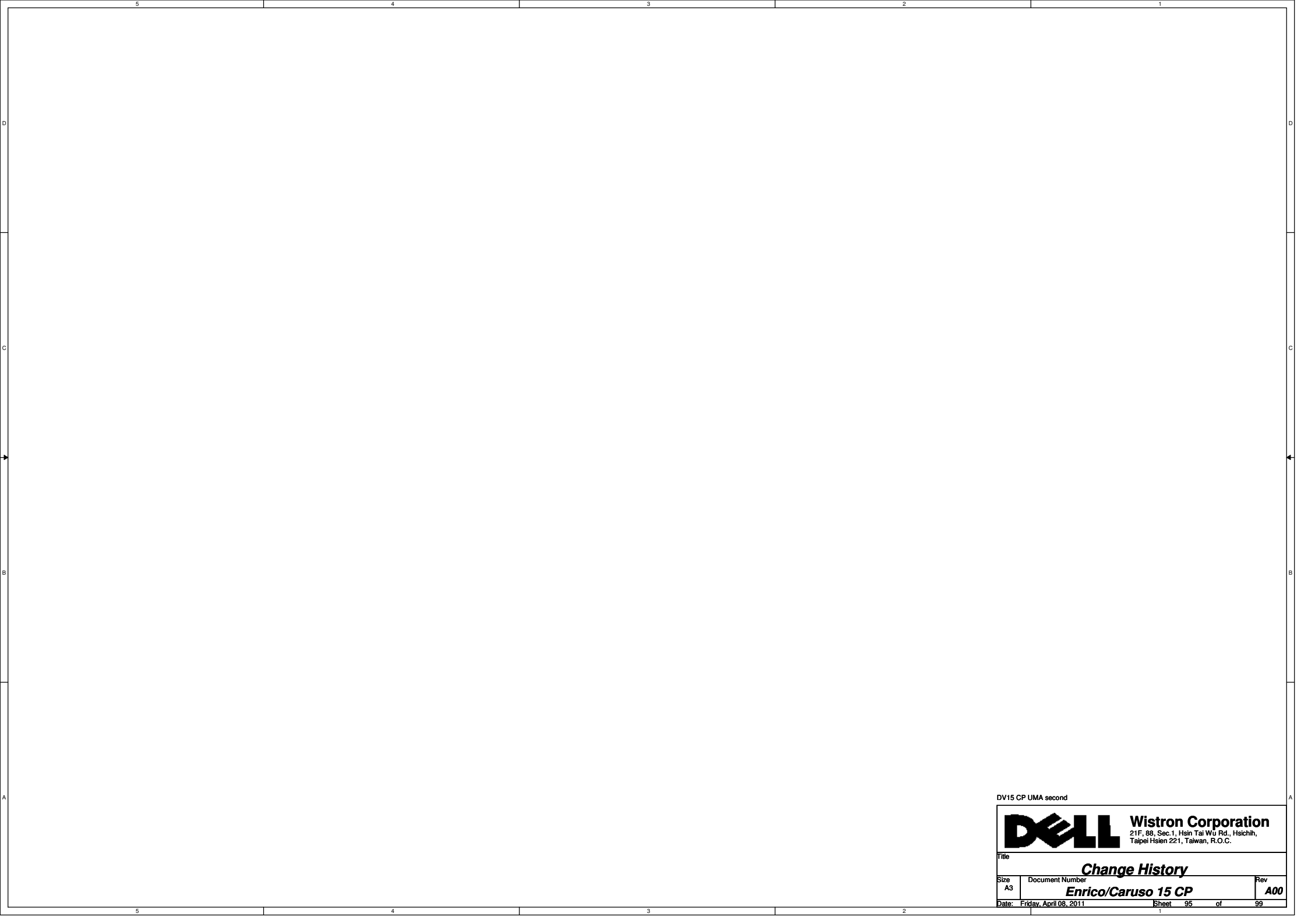
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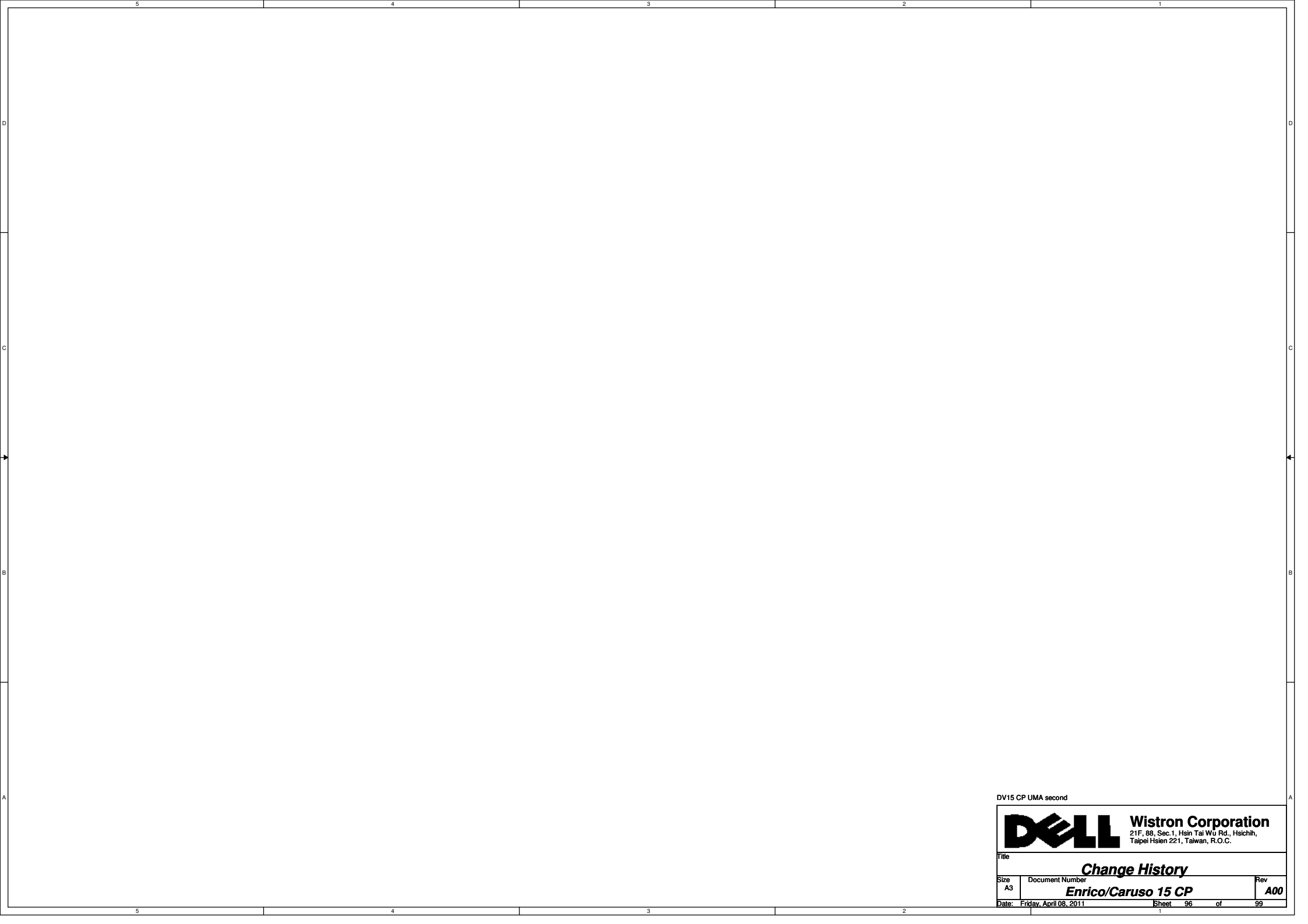
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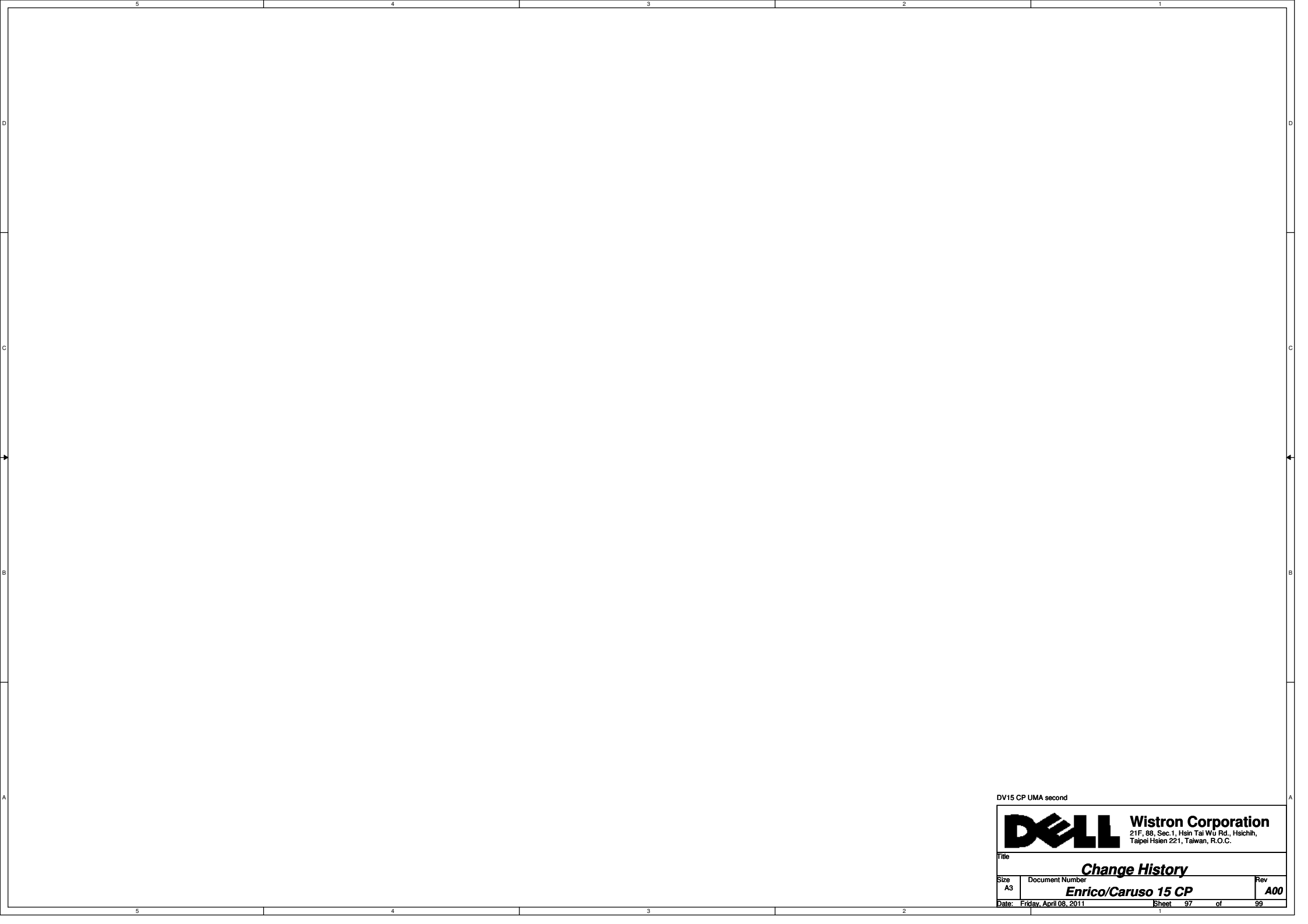
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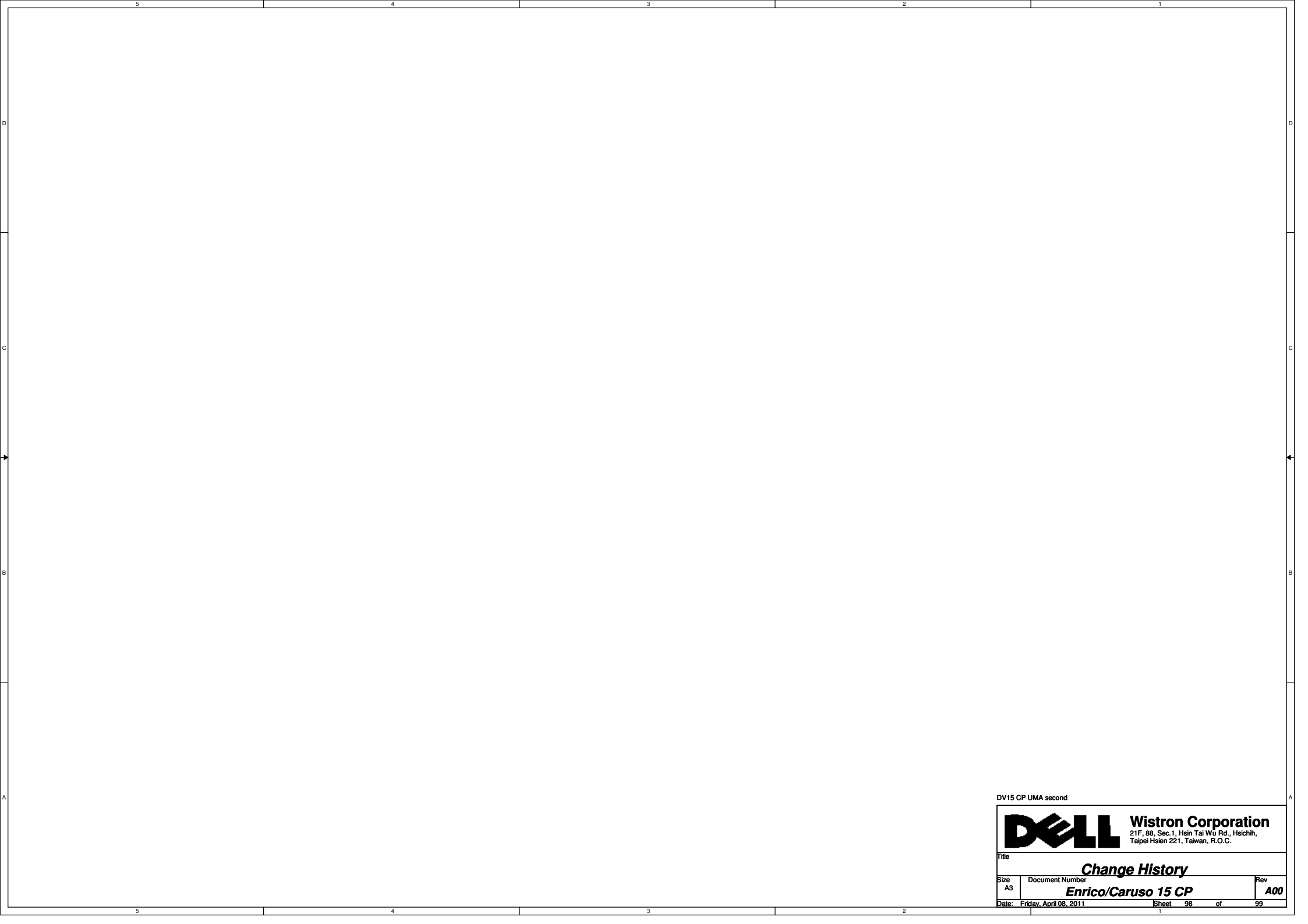
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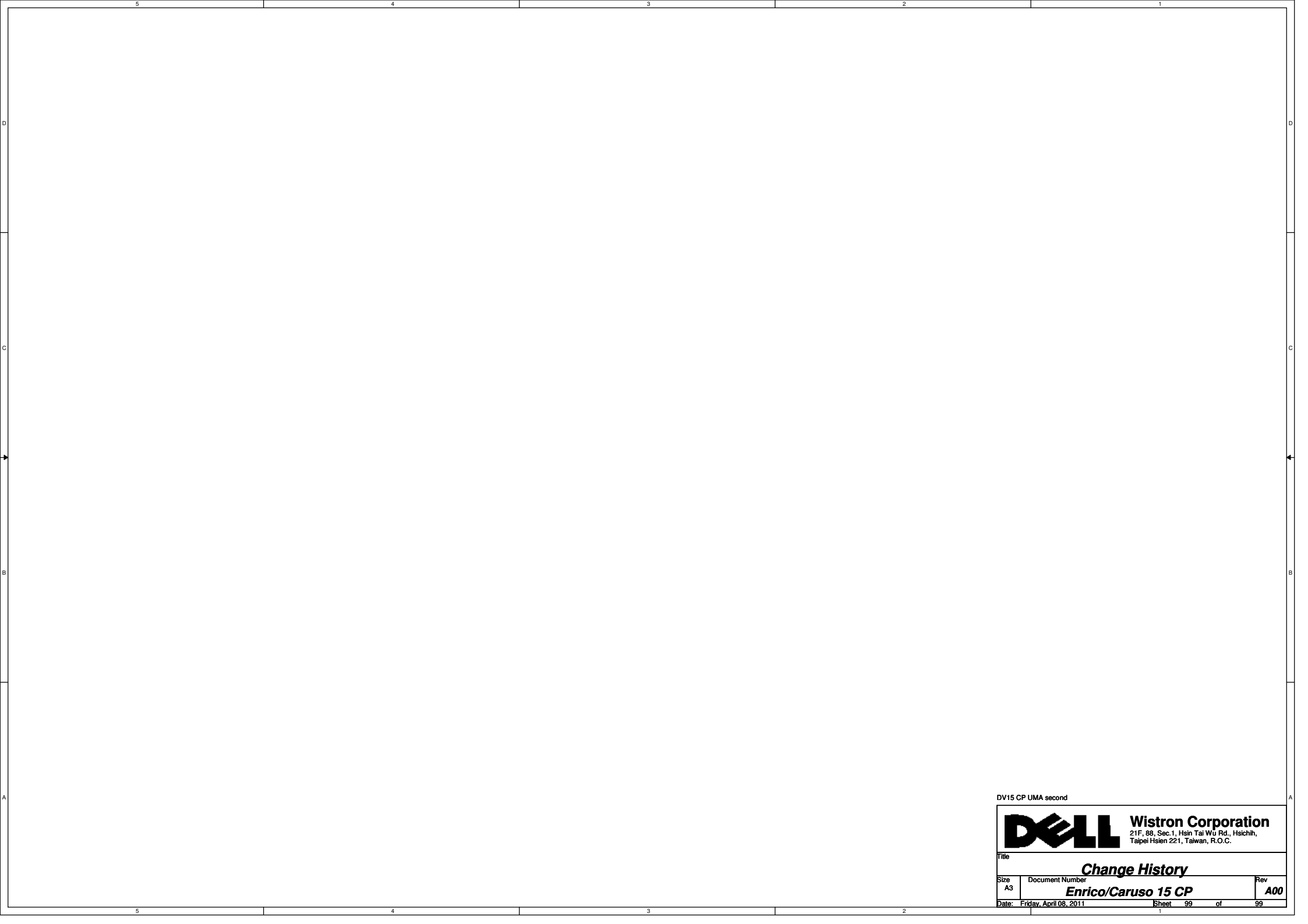
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